Sean Owen Clancy, Ph.D.

Failure Analysis Techniques

for Electronics

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1. Introduction

ACI Technologies, Inc. (ACI) offers competitively priced and prompt analysis and testing of bare boards, components, and assemblies. Reliable failure analysis requires a full range of analytical equipment, along with trained and experienced personnel to accurately interpret the data and develop recommendations to resolve the circumstances that lead to the issue.

ACI's manufacturing facility connects years of manufacturing experience with the industry's newest and most advanced electronics manufacturing equipment. This allows ACI analytical service engineers to understand how changes in the manufacturing process affect product performance and reliability. This facility also gives ACI the ability to manufacture samples, verify material selection, or duplicate any aspect of the electronics manufacturing process. ACI engineers and process consultants work closely with board and substrate fabricators, component manufacturers, and assemblers to improve product quality, reduce risk, and provide solutions for electronics manufacturing challenges. Work is performed to IPC, IEEE, ASTM, JEDEC, and MIL-SPC standards.

The highly skilled engineers at ACI are happy to assist our customers with open communication, problem assessments, quotations within 24 hours, and reliable results. Both standard and expedited testing are available, and the option of onsite problem review and assessment. Quantity discounts are available.

Figure 1-1: ACI is conveniently located in a modern office park adjacent to the Philadelphia International Airport.

2. Analytical Services

The analytical services laboratory at ACI provides a full range of solutions tailored for the electronics manufacturing industry. Using experienced electrical, materials, process and manufacturing engineers and scientists, ACI performs detailed investigations in the areas of materials analysis, electrical characterization, and device integrity. Our environmental stress screening and harsh environment testing methods can offer crucial information about product reliability. All testing is conducted in accordance with IPC, JEDEC, ASTM, Belcore, and MIL-STD specifications. The ACI advantage provides quick and accurate results and also root cause analysis and recommendations on how to prevent reoccurrence.

The following is a list of ACI's analytical services capabilities and serves as the basis for the organization of this document:

- Failure Analysis
  - Decapsulation/Delidding
  - Dye and Pry Testing
  - Microsectioning
  - Qualification of Bare Boards and Assemblies
- Imaging
  - Automated Optical Inspection
  - Endoscopic Optical Inspection
  - Optical Microscopy with Digital Imaging
  - Metallography with Digital Imaging
  - Scanning Electron Microscopy (SEM) with Energy Dispersive X-Ray Spectroscopy (EDS)
  - Transmission X-Ray Imaging and Inspection
- Cleanliness Testing
  - Bulk Ionics/Ionograph Testing
  - Ion Chromatography
  - Residual Rosin Testing
  - Surface Organic Contamination Detection Testing
  - Surface Organic Contamination Identification Testing
  - Surface Insulation Resistance (SIR) Testing
- Solderability Testing
  - Accelerated Steam Aging
  - Dip and Look
  - Solder Float Test
  - Wetting Balance
  - Sequential Electrochemical Reduction Analysis (SERA)

2. Analytical Services

- Spectroscopic Analysis
  - Energy Dispersive X-Ray Spectroscopy (EDS)
  - Fourier Transform Infrared (FTIR) Spectroscopy
  - Ultraviolet/Visible (UV/Vis) Spectroscopy
  - X-Ray Fluorescence (XRF) Spectroscopy
- Thermal Analysis
  - Differential Scanning Calorimetry (DSC)
  - Thermal Gravimetric Analysis (TGA)
- Wire Bond Mechanical Testing
  - Ball Wire Bond Shear Testing
  - Wire Bond Pull Testing
  - Non-Destructive Wire Bond Pull Testing
  - Die Shear Testing
- Non-Destructive Testing
  - Cleanliness Examination
  - Visual Examination
  - X-Ray Examination
  - Mechanical Examination
- Counterfeit Component Screening
- Solder Analysis
- Environmental Stress Screening (ESS) Testing
  - Highly Accelerated Stress Testing (HAST)
  - Mechanical Drop Shock Testing
  - Salt Fog Chamber Testing
  - Temperature/Humidity Cycling
  - Thermal Cycling
  - Thermal Shock
  - Vibration/Mechanical Testing

3. Failure Analysis

ACI offers the following testing for determining the failure mechanisms and root cause of issues that may arise. The subsequent sections expand on ACI's capabilities through which we are able to identify and resolve manufacturing issues.

3.1. Decapsulation/Delidding

Decapsulation is the removal of the plastic encapsulant to expose the underlying circuitry, carefully using nitric and sulfuric acids.

Delidding is the removal of a lid on a metal or ceramic package to expose the underlying circuitry, using acids to remove the seal or mechanically prying the package open.

The die, metallization, and wire bonds are observed after exposing the circuitry, as well as examined for possible failure mechanisms, such as electrical overstress (EOS) and electrostatic discharge (ESD).

Figure 3-1 shows a decapsulated component in which the wire bonds were examined.

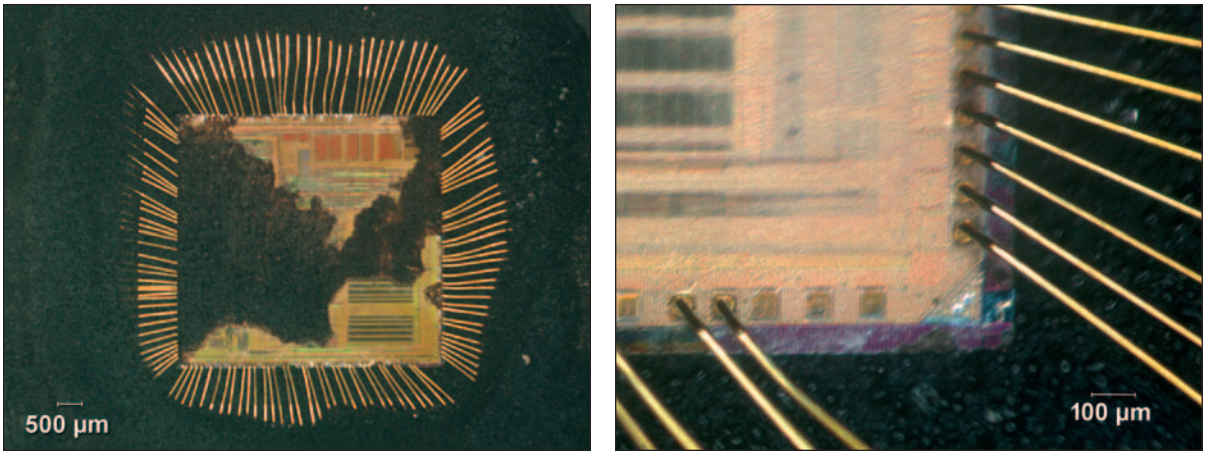


Figure 3-1: Images of a partially decapsulated component with close up of wire bond locations.

3.2. Dye and Pry Testing

Dye and pry testing involves immersing a ball grid array (BGA) component sectioned from an assembly into a dye solution. After immersion, application of vacuum, and drying, the device is pried apart and examined optically to see if cracks or other solder joints failures are present.

Figure 3-2 shows a couple of solder balls from a BGA assembly that had dye stains on interface between the component's solder ball to board. Having dye present in these locations indicate that there was a poor or damaged solder joint.

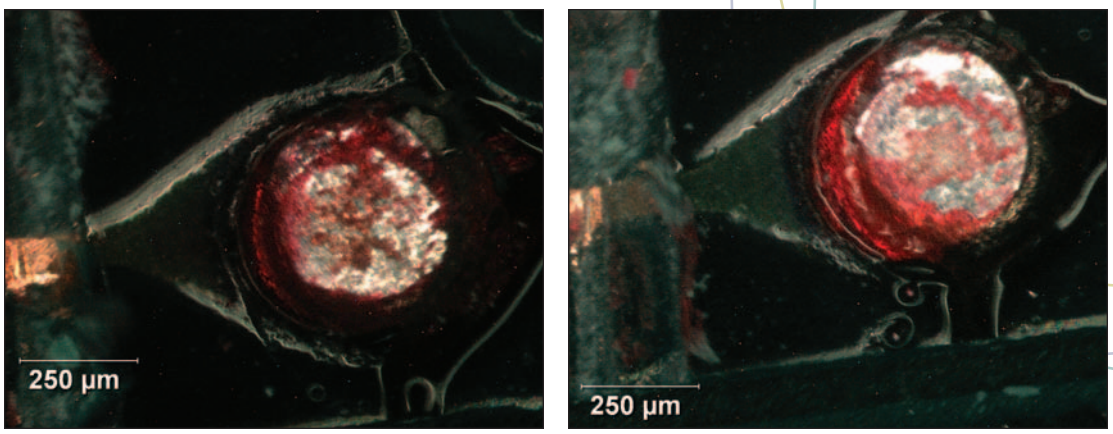


Figure 3-2: Images of dye on individual solder balls from an assembly.

3.3. Microsectioning

Microsectioning of components, bare boards, and assemblies is performed in accordance to *IPC-TM-650 2.1.1E - Microsectioning, Manual Method*. Microsectioning, by its definition, is a destructive technique from which information about the internal construction of a sample is obtained, and is necessary for qualification of bare boards and finished assemblies to IPC specifications, *IPC-A-600 (latest revision) - Acceptability of Printed Circuit Boards* and *IPC-A-610 (latest revision) - Acceptability of Electronic Assemblies, respectively*.

Figure 3-3 shows a plated through hole (PTH) of a microsectioned bare board with measurements of copper plating features internal to the board.

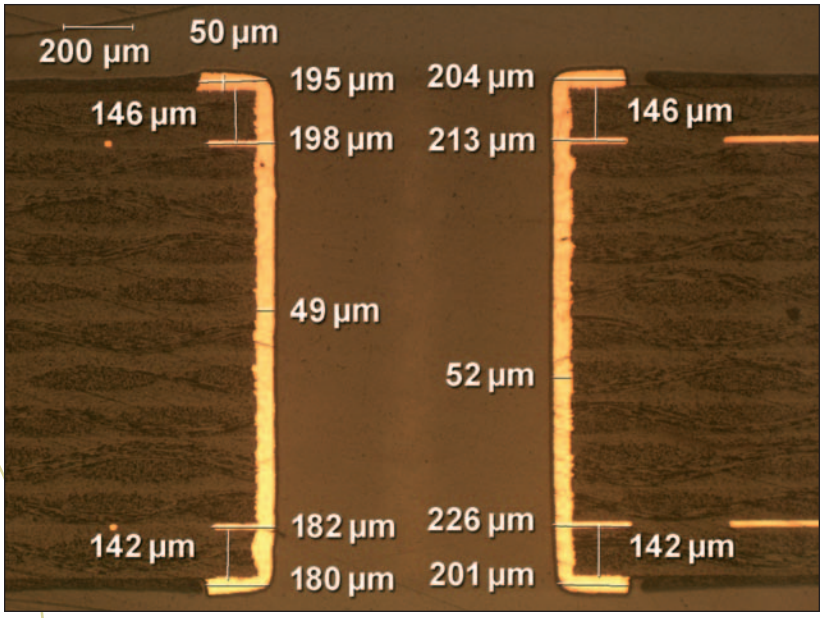


Figure 3-3: Metallographic image of microsectioned bare board with copper plating and foil measurements.

3.4. Qualification of Bare Boards and Assemblies

Qualification of bare boards is performed in accordance to *IPC-6012 (latest revision) - Qualification and Performance Specifications for Rigid Printed Boards* and *IPC-A-600 (latest revision) - Acceptability of Printed Circuit Boards*, in Class 1, 2, and 3, with Class 3 designed for the highest reliability for use in aerospace, defense, and medical device industries. The types of analysis include:

- visual examination of surface features and finishes using optical microscopy,
- thickness measurements of surface finishes using X-ray fluorescence (XRF) spectroscopy,
- microsectioning the board and evaluating the internal construction, and using scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM-EDS) to examine the elemental composition of features along with high magnification imaging.

Qualification of bare boards is performed in accordance to *IPC-6012 (latest revision) - Qualification and Performance Specifications for Rigid Printed Boards* and *IPC-A-610 (latest revision) - Acceptability of Electronic Assemblies*, in Class 1, 2, and 3, with Class 3 designed for the highest reliability for use in aerospace, defense, and medical device industries. The process uses the same types of analysis as for bare boards and includes evaluation of solder joints.

3.5. Failure Analysis Case Studies

Case studies of the more common failures ACI has observed are discussed in this section and include:

- Head-on-Pillow
- Solder Voiding
- Pad Cratering
- Surface Finish Issues
  - Porous or Thin Gold Layer over Nickel
  - Black Pad
  - Gold Embrittlement
- Corrosion Products

3.5.1. Head-on-Pillow

The head-on-pillow defect is an instance in which both the paste deposit and the solder bump reached a full state of melt, but failed to coalesce. The origin of head-on-pillow is a barrier preventing the coalescence of the solder bump and solder paste deposit. The reflow profile can be a source of head-on-pillow defects by exposure of the flux to excessive temperatures causing the flux to exhaust its oxidation cleaning abilities prior to the conclusion of the reflow cycle. A process modification made to prevent this occurrence is to reduce the profile length and/or modify the profile temperatures to avoid the premature exhaustion of the flux. The use of an inert atmosphere, such as nitrogen, may mitigate head-on-pillow defects by hindering oxide formation on the solder bumps after the flux is exhausted during the reflow cycle.

An additional cause of head-on-pillow is an insufficient volume of solder paste (and thus flux). Excess oxidation can prevent homogeneity between the solder ball and the solder paste deposit; therefore optimization of the solder paste printing process is required to ensure sufficient paste is present.

The barrier may also be due to a contamination on the surface of the solder bump that flux in the solder paste is not able to remove. Analysis for the presence of contamination may require an extraction method appropriate for non-ionic detection, such as FTIR spectroscopy. If no contamination is observed on raw materials in as-received condition, a thorough assessment of the handling practices is necessary. Testing to ensure that the components are not entering the facility with the suspect contaminant is an essential primary action. Control of solder paste materials such as proper storage and handling and observance of shelf life control, storage conditions, factory environmental conditions, and stencil life performance are essential.

Head-on-pillow typically results as an intermittent open connection. An assembly showing this condition may be corrected through BGA rework process which includes: BGA removal, cleaning of the board pads, and resoldering either: (1.) a new component or (2.) the removed component that has been re-balled. New solder paste can be placed at the board location using a mini-stencil, however this is a difficult process. Another alternative is to only apply tacky flux to the pads prior to resoldering the component.

Figure 3-4 shows the head-on-pillow condition of a BGA solder joint in a microsectioned assembly.

Figure 3-4: Metallographic image of a head-on-pillow defect on a BGA assembly.

3.5.2. Solder Voiding

IPC-A-610E specifies voiding that exceeds 25% of the X-ray image area is a defect for all classes of production. ACI recommends that any voiding that exceeds 10% of the ball X-ray image area be treated as a process related process indicator condition (i.e., a condition that indicates excessive variation from the intended result but is not specifically defined as a process indicator in the assembly standards).

The location of voids in a BGA solder joint can be critical, regardless of the size of the void(s). Voids that occur at the solder joint/printed circuit board (PCB) land interface ("interface voids") can impact the reliability of the resulting solder joints. This occurs because the yield strength of a solder joint is related to the surface area of contact between the solder and the surfaces it joins. Interface voids reduce this contact area and thus can lead to mechanical failure of the solder joint.

Voiding can be a result of varying causes which include the properties of the flux used on the assembly and the profile used to reflow the solder paste. Interface voids can also be a result of non-wetting to or dewetting from the PCB land. Figure 3-5 shows an X-ray image of voids in the solder joints of a BGA assembly. Figure 3-6 shows a cross-sectional view of solder voids observed in a BGA.

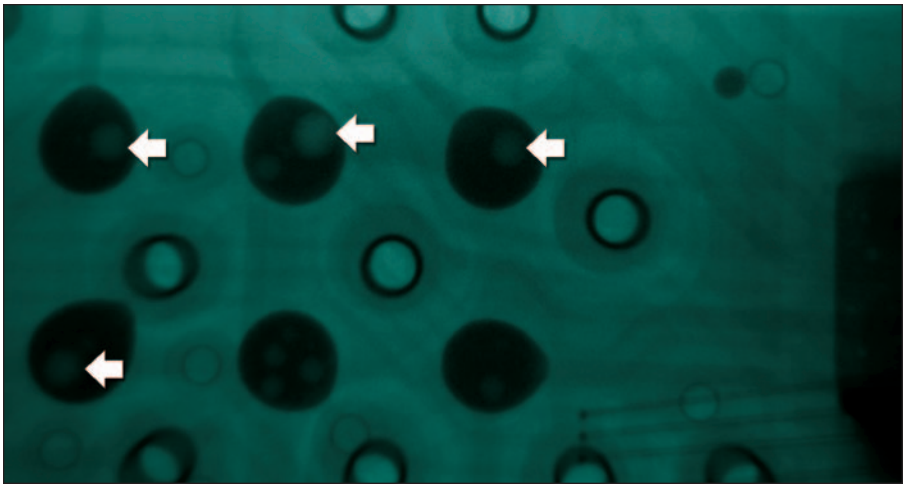


Figure 3-5: X-ray image of voids in the solder joints of a BGA assembly.

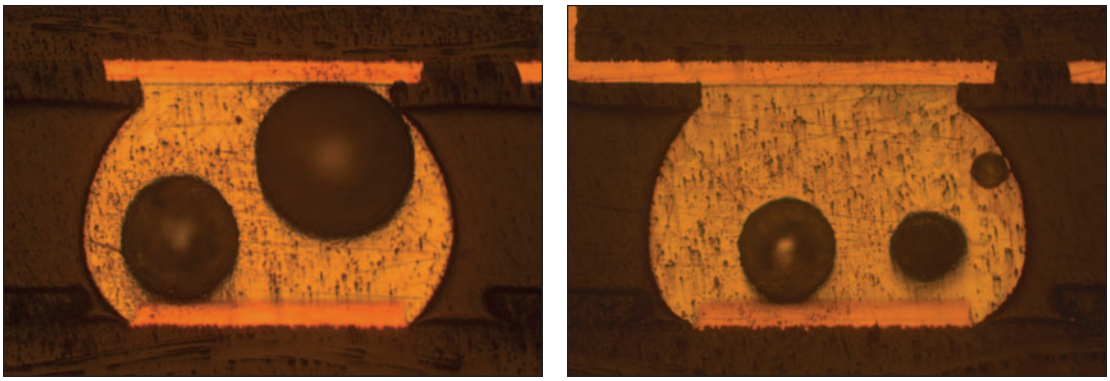


Figure 3-6: Metallographic images of voids observed within solder balls on a BGA assembly.

3.5.3. Pad Cratering

Fracturing of the resin layer under solder lands is a condition known as pad cratering. The path of the fractures may comprise connecting traces or vias, resulting in a breach which in time would lead to an electrical failure. Pad cratering is a sign of mechanical stress in excess of the limits of the material used in the PCB and is more typically observed in lead-free assemblies.

3. Failure Analysis

In Figure 3-7, the proximity of the solder joint fracture to a pronounced fracture of the laminate indicates the stresses causing the cratering likely created the separation in the solder joint. In fact, the metallurgical structure of the fractured solder joint are consistent with a well controlled lead-free soldering process, which further strengthens the conclusion that the solder fracture is an effect that resulted from the pad cratering that was observed. Examination of the failed assembly confirmed pad cratering occurring on both sides of the assembly. This particular occurrence did not appear be the root cause of the board failure, but was considered to be indicative of similar circumstances occurring elsewhere on the assembly in which a complete separation at the junction of solder ball to pad had occurred.

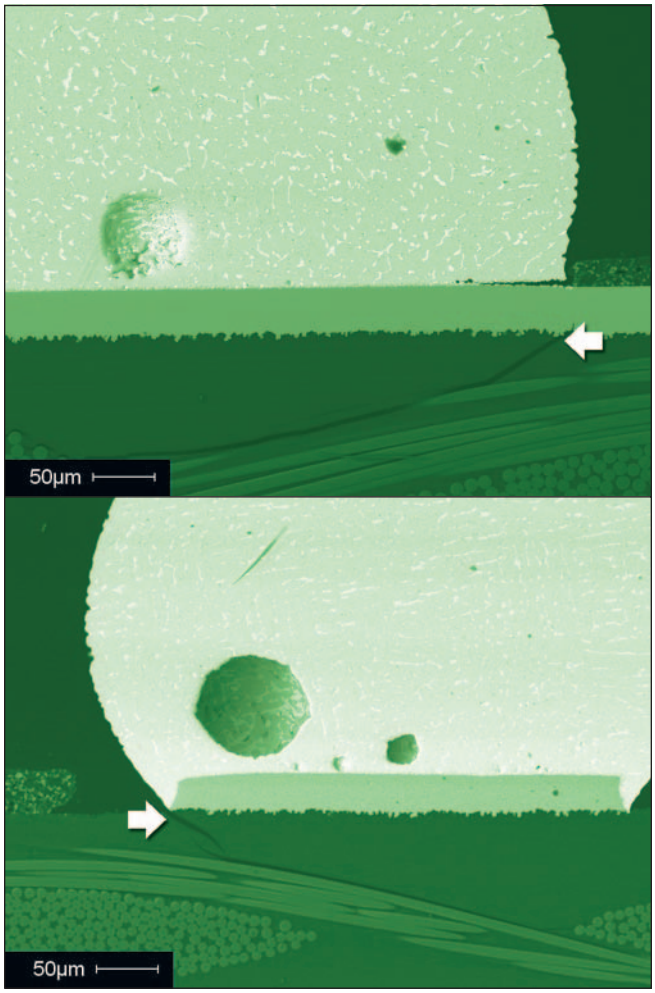


Figure 3-7: SEM images displaying fractured laminate beneath the pads of the soldered component.

Pad cratering is more common at BGA locations for a number of reasons. A BGA solder joint does not have inherent stress relief as is found on a gull wing lead connection. BGA solder lands typically have a low individual surface area. Many components, such as large BGAs, are more susceptible to damage due to vibration (due to high mass) or deflection of the substrate (due to high footprint area) than smaller components.

Prevention of pad cratering requires actions that either reduce the stress on the interconnect site or mitigate the effects of stress. Reducing stress may require changes to the layout of the PCB or design of the overall assembly the PCB is used in. Adhesives may be used to provide additional mechanical strength but may not prove to be sufficient in some situations. Adhesives can be applied as underfills or as external package perimeter bonding.

Changes to the material specification for the PCB laminate can also be an effective strategy to prevent pad cratering. The material composition (fillers) and fabrication methods (cure process) required changes to increase the thermal resistance and dimensional stability in laminates for lead-free processing. These changes also tend to increase the propensity for pad cratering, especially when coupled with the lead-free solders used today.

IPC-4101C - Specification for Base Materials for Rigid and Multilayer Printed Boards requires the laminate material to conform to a minimum trace peel strength specification, but the minimum requirements may not be sufficient for all designs and service environments. Peel strength testing per *IPC-TM-650 Method 2.4.8C - Peel Strength of Metallic Clad Laminates, Condition A: As Received* can be used as a comparative test between different laminate materials. Peel strength testing per *IPC-TM-650 Method 2.4.8C - Peel Strength of Metallic Clad Laminates, Condition B: After Thermal Stress* can be used to compare laminate materials after exposure to thermal stress that simulates soldering processes. Samples for testing should be sourced from qualified PCB suppliers and can be as provided in *IPC-TM-650 Method 5.8.3 - Peel Strength Test Pattern* or Coupon C or N from *IPC-2221A - Generic Standard on Printed Board Design*.

Peel strength testing should also be performed periodically by PCB suppliers to ensure their “as received” laminate is in compliance with applicable specifications and to ensure the PCB fabrication process does not degrade the laminate and increase the likelihood of pad cratering on the completed assembly.

3.5.4. Surface Finish Issues

A surface finish is required on a printed circuit board (PCB) to cover the exposed copper with a material that will protect the copper from oxidation and corrosion, as well as provide a solderable surface that ensures a reliable solder joint. There are a variety of choices in surface finishes; each has its own advantages and disadvantages. The most common types of surface finishes are:

- Electroless Nickel Immersion Gold (ENIG)
- Immersion Silver (IAg or ImAg)
- Immersion Tin (ISn or ImSn)
- Organic Solderability Preservative (OSP)
- Hot Air Solder Leveled (HASL)

Each of the surface finishes requires control of the deposition processes in order to provide a quality product. When the process falls out of control specifications, problems can arise in the final assembly in the form of weak solder joints. The following sections describe cases that resulted from when gold is too thin, an occurrence of black pad, and when gold is too thick.

Table 3-1 provides a comparison of the properties of the more common surface finish types.

Border Finish	Positives	Negatives
Electroless Nickel Immersion Gold (ENIG)	• Good corrosion resistance for on-board contact pads • Suitable for wire bonding pads • Good co-planarity features • Excellent board shelf life	• Cost • Gold embrittlement possible with gold finished components • Black pad caused by corrosion of the nickel layer during plating
Immersion Tin (ImSn)	• Good co-planarity features	• Tin thickness control • Tin whiskers potential on unsoldered tin plated pads • Limited board shelf life
Immersion Silver (ImAg)	• Good co-planarity features • No AgCu reaction	• Cost • Environmental storage requirements • Board tarnishing
Organic Solderability Preservative (OSP)	• High volume, low cost alternative • Good co-planarity features	• Solderability degrades after multiple reflows • "Halo" effect around solder joints from OSP finished pads • Board finish may interfere with in-circuit test points • In-circuit test plan may need to be re-evaluated
Hot Air Solder Level (HASL)	• Excellent solderability ("nothing solders like solder")	• Difficult to control finishing process • Co-planarity a major problem for fine pitch applications

Table 3-1. Comparison of surface finish properties.[1]

3.5.4.1. Porous or Thin Gold Layer over Nickel

A customer submitted an assembly that was exhibiting intermittent opens at multiple locations on a BGA component. The assembly's functionality did not survive international shipping, essentially shock and vibration failures, immediately making the quality of the solder joints suspect. The customer was asked about the contract manufacturer and the reflow oven profile as well as the solder paste and surface finish used. The ACI engineering staff evaluated the contract manufacturer's technique and determined that they were competent in the methods they used for placing thermocouples in the proper locations and developing the reflow oven profile. The surface finish was unusual, but not unheard of, in that it was hard gold over hard nickel, rather than electroless nickel immersion gold (ENIG). The customer was able to supply boundary scan testing data which showed a diagonal row of troublesome BGA pins.

[1] Partee, Blaine. "Lead-Free Conversion: Surface Finishes." *EMPFasis*. EMPF, 1 March 2006. Web, 16 August 2011. <http://www.empf.org/empfasis/2006/mar06/lfconversion.html>.

The ACI analytical services staff determined that cross-sectional analysis with optical microscopy and scanning electron microscopy (SEM) with energy dispersive X-ray spectroscopy (EDS) would provide the best information as to what had happened. The focus of the microsectioning was through the diagonal row of the BGA pins indicated by the boundary scan data.

A position halfway through the BGA solder balls along a diagonal through the BGA component was selected as the area of interest to examine the solder joints, surface plating, and foil thickness as well as any anomalies from internal observations. The microsectioning was performed in accordance with *IPC-TM-650 2.1.1 - Microsectioning, Manual Method*. In Figure 3-8, images of one of the suspect solder joints are shown with a clean break along the board pad to solder ball interface.

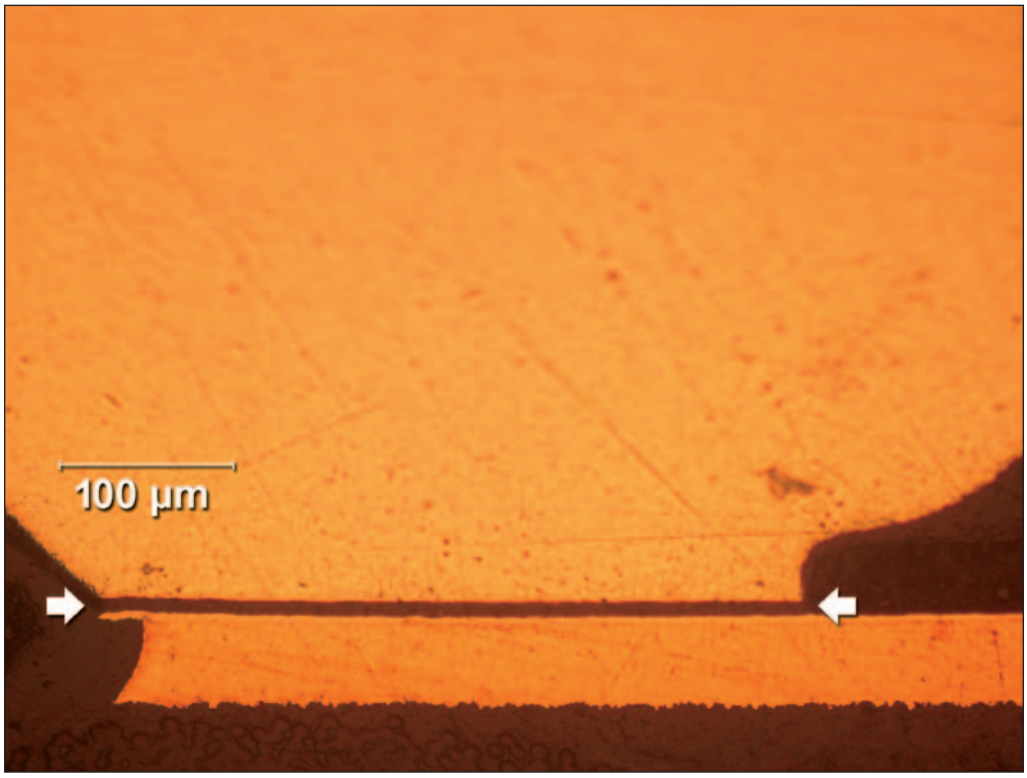


Figure 3-8: Metallographic image of a broken solder joint along the board pad to solder ball interface.

After examining similar solder joint cracks under optical microscopy, the cross-section was analyzed using SEM-EDS. Figure 3-9 shows the pad interface of the cracked joint of an outer BGA solder ball in which nickel (Ni) was predominant with a minor contribution of tin (Sn). Figure 3-10 shows the solder ball interface of the same cracked joint of an outer BGA solder ball with copper (Cu) from the SAC (SnAgCu) solder paste, nickel (Ni) from the pad, gold (Au) from the pad, and tin-silver (SnAg) from the solder ball.

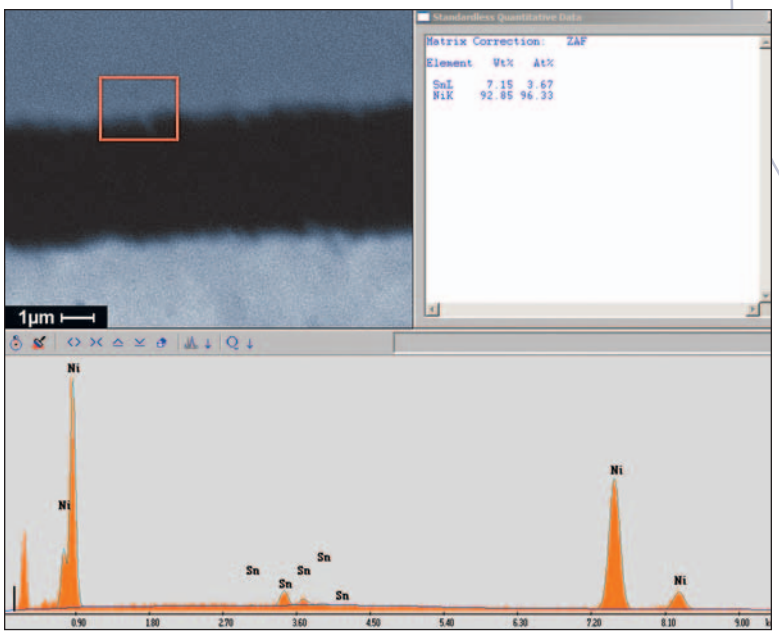


Figure 3-9: SEM-EDS data for the pad side of an outer solder joint that cracked.

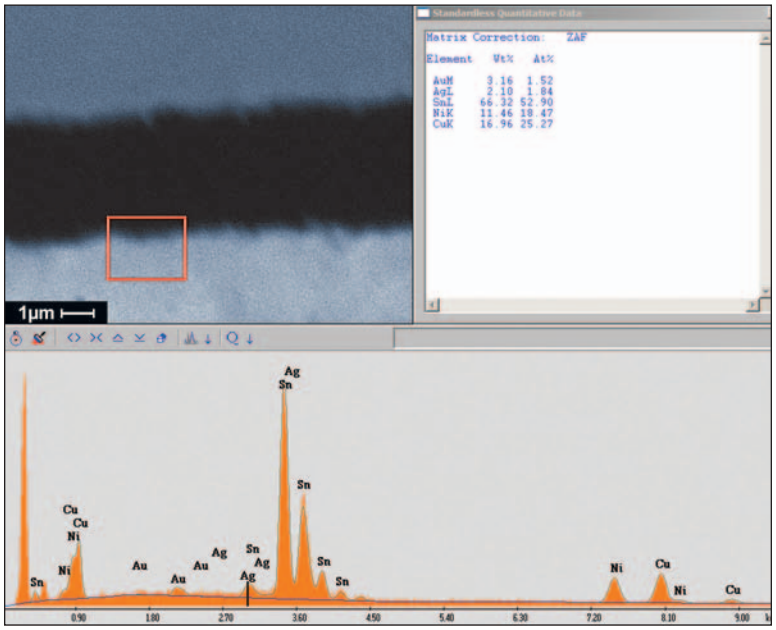


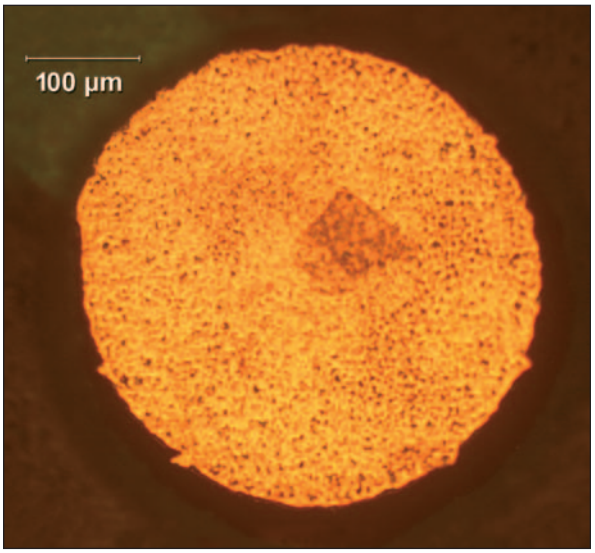
Figure 3-10: SEM-EDS data for the solder ball side of an outer solder joint that cracked.

The low levels of gold observed at the interface, especially with no line of demarcation, and few intermetallics at the pad interface (with the hard gold over hard nickel plating) suggested that there was an issue with the bare board. Oxidation of the nickel plating, either during the surface finish deposition or through an insufficient layer of gold, could prevent solder from adhering to the pad to form a strong solder joint. The patchy intermetallic layer observed at the interface also suggested a blocking of the nickel interface.

The clean breaks at the nickel layer of some of the BGA solder joints, especially from the outside towards the inside of the component, indicated that it was less likely the assembly manufacturing process was the cause and more likely the bare board. During the reflow process, the corners of the component are the hottest and the center should be coldest. The center would most likely fail if the process was too cold while dewetting and excessive intermetallics would be observed if the process was too hot. These observations pointed to the surface finish as the likely problem since low intermetallic formation was observed and the solder joints weren't broken near the center of the BGA.

ACI recommended evaluating the plating process of the bare board and the hard gold over hard nickel surface finish to see if they met the recommended thicknesses for the nickel and especially the gold layers. Also, removal of any storage or processing step that would have led to the oxidation or fouling of the nickel surface should increase the solder joint reliability.

Optical microscopy, X-ray fluorescence (XRF) spectroscopy, and/or SEM-EDS techniques were recommended to determine the plating thickness and porosity. The customer was able to provide a bare board from a similar lot to the previously examined assembly. Figure 3-11 shows the uneven and apparently porous gold surface of a representative BGA pad location. Figure 3-12 shows the SEM-EDS elemental mapping for a BGA pad where nickel appears to be visible through thin patches of the gold plating. All of this data indicates that the process producing these boards was not properly controlled.



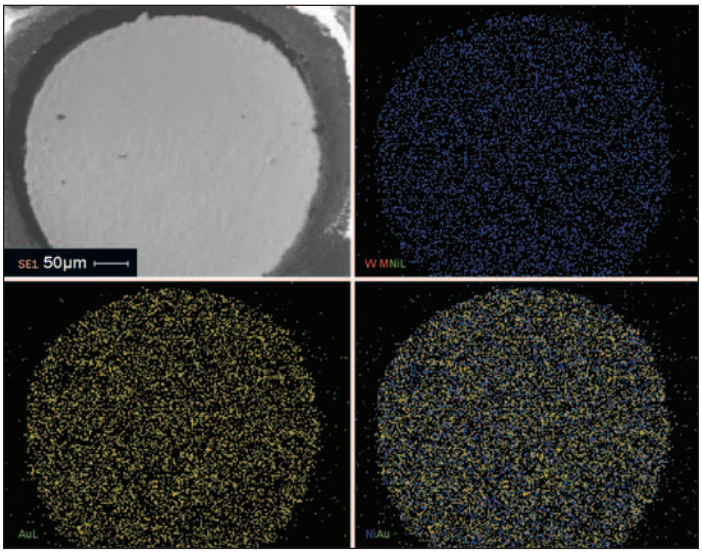


Figure 3-11 (above left): Optical image of the rough surface of a pad.

Figure 3-12 (above right): SEM-EDS elemental map of a pad. Top left - image, top right - nickel (blue), bottom left - gold (yellow), bottom right - overlay of both. The overlay map shows patches where the nickel may be exposed through the gold.

ACI recommended that the customer speak with their bare board manufacturer about improving the hard gold over hard nickel plating process or switching to other surface finishes, such as soft gold over nickel plating, electroless nickel immersion gold (ENIG), or immersion silver (IAg).

3. Failure Analysis

The customer made a new set of boards with an IAg surface finish and provided them to the ACI in the bare board and finished assembly states. Figure 3-13 shows images of a representative solder joint in which good bonding along the board pad to solder ball interface was observed.

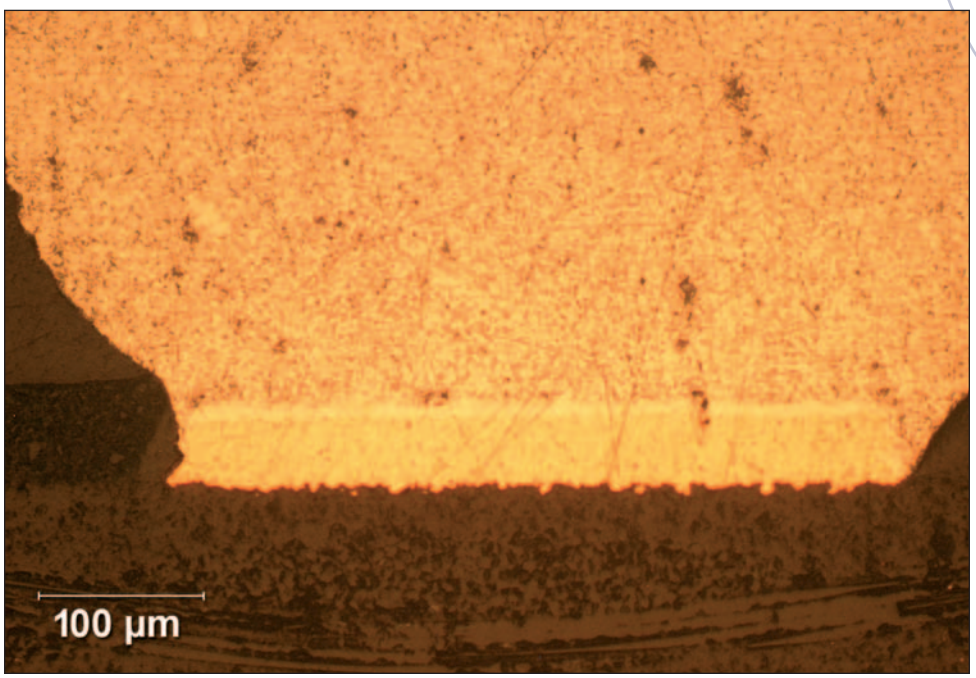


Figure 3-13: Metallographic image of a good solder joint along the board pad to solder ball interface.

ACI recommended that the customer perform incoming quality acceptance inspections on PCBs as part of their supplier quality control strategy until such time that the supplier has proved capable of providing material acceptable to the appropriate requirements. The acceptance testing should include solderability testing, non-destructive plating thickness measurement, and visual workmanship assessment to ensure compliance to the requirements of *IPC-6012 - Qualification and Performance Specification for Rigid Printed Boards* and *IPC-A-600 - Acceptability of Printed Boards*. Failure to meet these requirements should be used as justification to reject individual PCBs and/or entire board lots, as necessary.

Additionally, the supplier should also perform inspections to ensure that nonconforming material is not provided to customer. The customer's drawings should place requirements on their supplier(s) by providing notes that use language similar to the following:

- Manufacture in conformance with the requirements of *IPC-6012 (latest revision)*, Class [1, 2, or 3, as appropriate].
- Inspect per the requirements of *IPC-A-600 (latest revision)*, Class [1, 2, or 3, as appropriate].

3.5.4.2. Black Pad

Black pad is a corrosion of the Ni layer during the immersion gold step of a ENIG surface finish. The end result can vary from complete dewetting of the pad/component surface to suitable wetting with weakened solder joints that do not often reveal themselves until after the device is in the field. As a result, routine *IPC-A-610* inspection efforts are not sufficient to screen for black pad.

There is some difference of opinion as to the black pad mechanism.[2,3,4] The end result is the same with either weakened solder joints or complete solder separation at the interface between either the solder and pad or solder and lead. The characteristic of a black pad failure, as the name states, is a blackened appearance of the pad surface, as seen in Figure 3-14. As a result of the variation in what is observed, the following is a list of characteristics that should collectively be observed to be considered a true black pad failure.

1. The fracture will occur at the solder-pad or solder-lead interface and not within the bulk solder.
2. Elevated levels of phosphorus at the fracture interface. It is known that at the IMC region, P levels do become naturally enriched. The difference with black pad is the Ni corrodes as a result of increased activity of the immersion gold step. This hyperactive immersion gold step is induced by pH, solder mask contamination, and the electric fields on the board.
3. Nickel on the surface of the PCB pad.
4. Mud cracks at the fracture interface and a lack of NiSn IMC compound as a result of the Ni being tied up as a NiP compound, as shown in Figure 3-15.

The difficulty in establishing a black pad mechanism stems from how the degree of Ni corrosion will influence what is observed. The corrosion, depending upon the degree and when it occurs could also influence the final thickness of the gold.

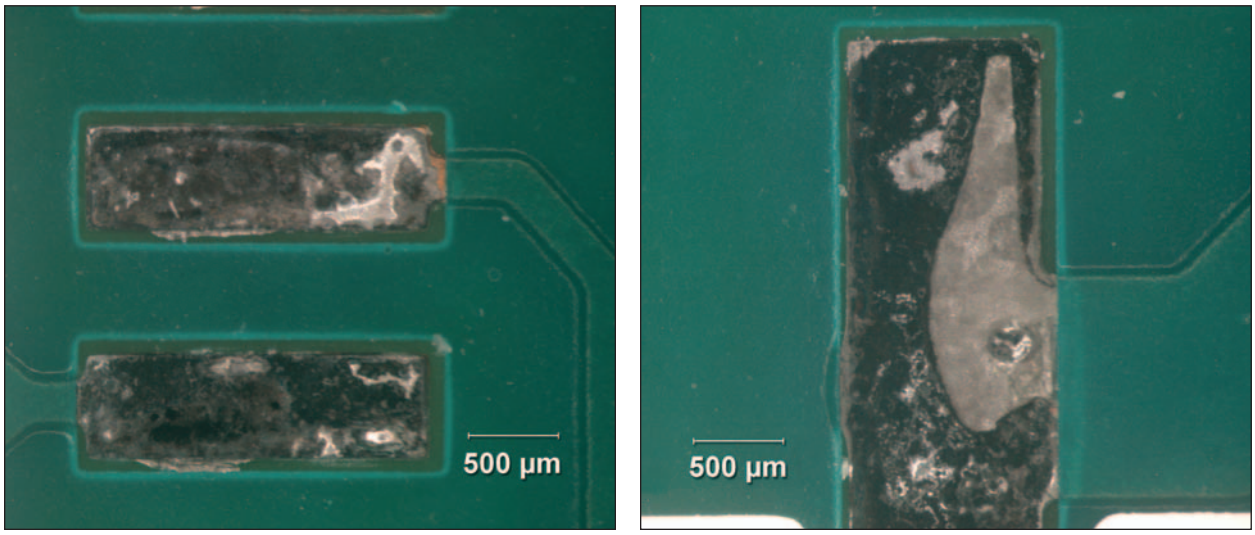


Figure 3-14: Images of black pad areas on multiple pads.

[2] Champaign, Robert F., Jodi A. Roepsch, and Marlin R. Downey. "Afraid of the Dark?" *Circuits Assembly*, Jan. 2003. Web. 3 May 2011. <http://www.circuitsassembly.com/pdf/0301/0301raytheon.pdf>.

[3] Houghton, F.D. Bruce. "Solving the ENIG Black Pad Problem: An ITRI Report on Round 2." *Printed Wiring Board Resource Center*. Web. 3 May 2011. <http://www.pwbrc.org/members/pdf/works99/Houghton.PDF>.

[4] Biunno, Nicholas. "A Root Cause Failure Mechanism for Solder Joint Integrity of Electroless Nickel/Immersion Gold Surface Finishes." *Sanmina-SCI*. Web. 3 May 2011. <http://www.sanmina-sci.com/Solutions/pdfs/pcbres/Blackpad_on_ENIG_Surface_Finishes.pdf>.

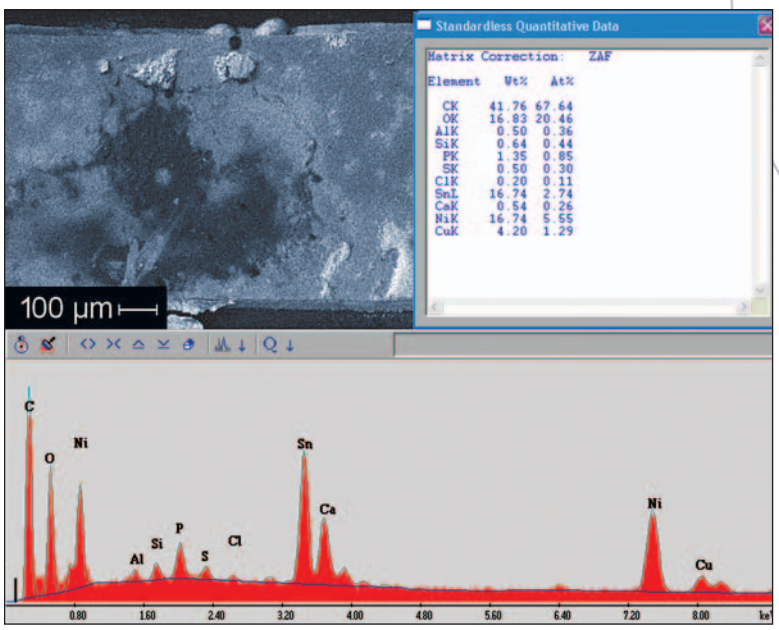


Figure 3-15: SEM-EDS data for a black pad area with mud crack morphology.

3.5.4.3. Gold Embrittlement

Electroplated gold can succumb to gold embrittlement since unlike ENIG, the amount of gold deposited is not self-limiting. Gold embrittlement is also a volume dependent phenomenon with embrittlement occurring at gold contents in the bulk solder greater than four to six percent.[5] During the final soldering operation, any remaining gold plating present on the surfaces being soldered, quickly dissolves into the bulk solder. The dissolved gold then combines with the tin component of the SnPb solder to form the intermetallics $AuSn_2$ and $AuSn_4$. When the gold and tin combine to form these intermetallics, voids form in the solder. An over-abundance of voids can create weakened areas of solder which can easily lead to cracking when exposed to mechanical stress, as seen in Figure 3-16. The gold-tin intermetallics first form needles, then blocks, and eventually can collect at the solder interfaces. An SEM image of intermetallic needles is shown in Figure 3-17.

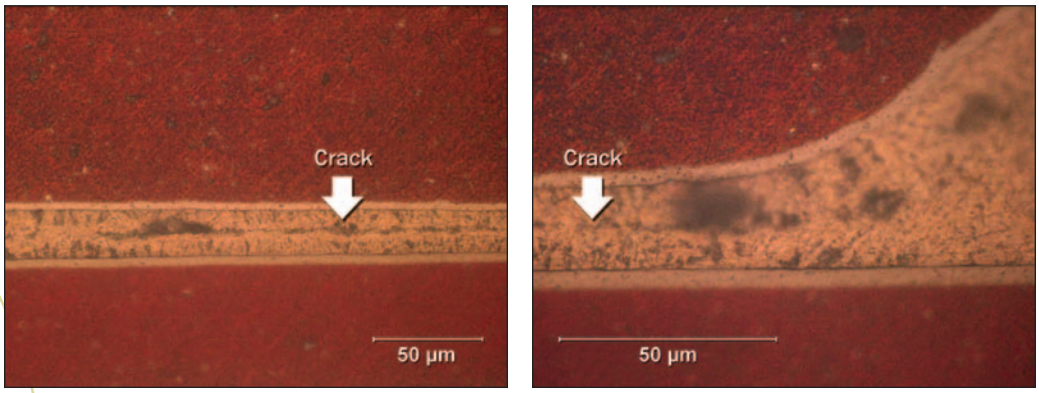


Figure 3-16: Metallographic images of a solder joint exhibiting gold embrittlement.

[5] Viswanadham, Puligandla, and Pratap Singh. *Failure Modes and Mechanisms in Electronic Packages*. New York: Chapman & Hall, 1998. Print.

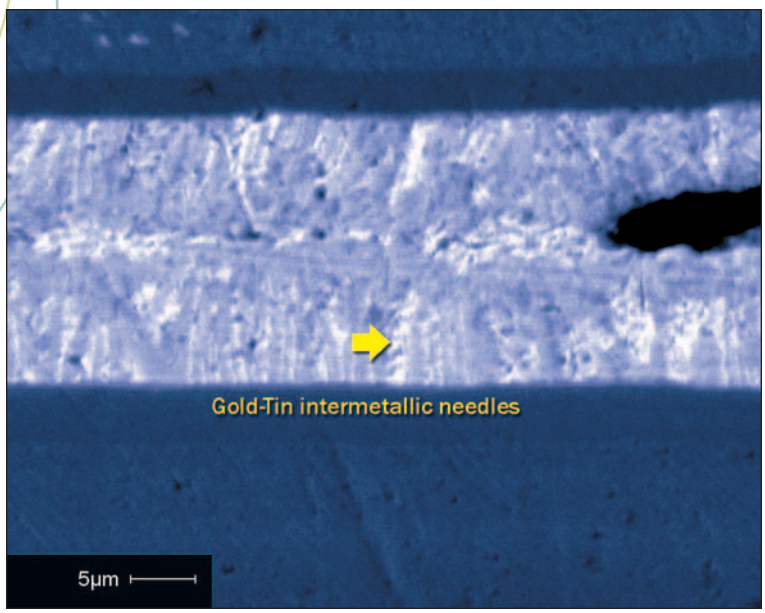


Figure 3-17: SEM image of a solder joint exhibiting gold embrittlement.

3.5.5. Corrosion Products

One of the most critical factors in preventing corrosion from occurring in electronics is maintaining the state of cleanliness. This is not an easy feat to achieve. Corrosion is defined as the deterioration of a material or its properties due to a reaction of that material with its chemical environment.[6] So, to prevent corrosion from occurring, either the material or the chemical environment must be adjusted. Adjusting the material usually means application of a protective coating or replacing a more reactive material with a less reactive material. Adjusting the chemical environment usually means removing ionic species through cleaning, and removing moisture, usually with a conformal coating or hermetic package. Ionic species and moisture are problematic because they form an electrolyte which is able to conduct ions and electricity. Any metal that comes into contact with the electrolyte can begin to corrode.

The most common source of corrosion on electronic assemblies is residual flux. Fluxes are specific chemistries applied during the soldering process which improve the wetting of the solder to both the pad and component when forming the solder joint. They can be highly reactive chemicals that, if left on the assemblies, can lead to corrosion, electrical degradation, and decreased reliability. In the presence of moisture and electrical bias, flux residue can enable dendritic growth as a result of electrochemical migration (ECM).

To establish the source of the corrosion products, the technical data sheets and materials safety data sheets (MSDS) can be used to help evaluate the chemistries of the approved fluxes. The cleaning process is also evaluated to assure the efficacy of cleaning the fluxes used in the manufacturing process. Furthermore, by establishing a correlation between the composition of the residues and the flux chemistries, one can eliminate or confirm the source of the corrosion. Analysis of the residues may be accomplished by employing scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM-EDS).

[6] Bob Stump National Defense Authorization Act for Fiscal Year 2003. Pub. L.107-314. 2 Dec. 2002. Stat. 116.2658.

3. Failure Analysis

Corrosion can be mitigated by preventing electrolytes from forming. This is accomplished by ensuring that any ionic residues are removed after the component, bare board, and assembly manufacturing, as well as preventing salts from depositing on the assembly from extreme environmental conditions. Moisture can be prevented on electronics assemblies by using a conformal coating or hermetic package. Also, materials selection in the design phase is important so that metals with dissimilar electrochemical potentials are not directly connected. If dissimilar metals must be used, such as when using specific surface finishes, like ENIG, then ensuring good bare board construction is a critical step in reliable, corrosion free electronics.

Figures 3-18, 3-19, and 3-20 show the corrosive effects of exposure to a sulfur-bearing environment. Figures 3-21 and 3-22 show an assembly exposed to a high-salt environment. Figure 3-23 show the effects of a high strength flux residue that did not include a cleaning process after assembly.

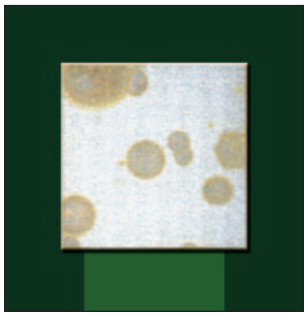


Figure 3-18: Areas of tarnish on a board with an immersion silver finish.

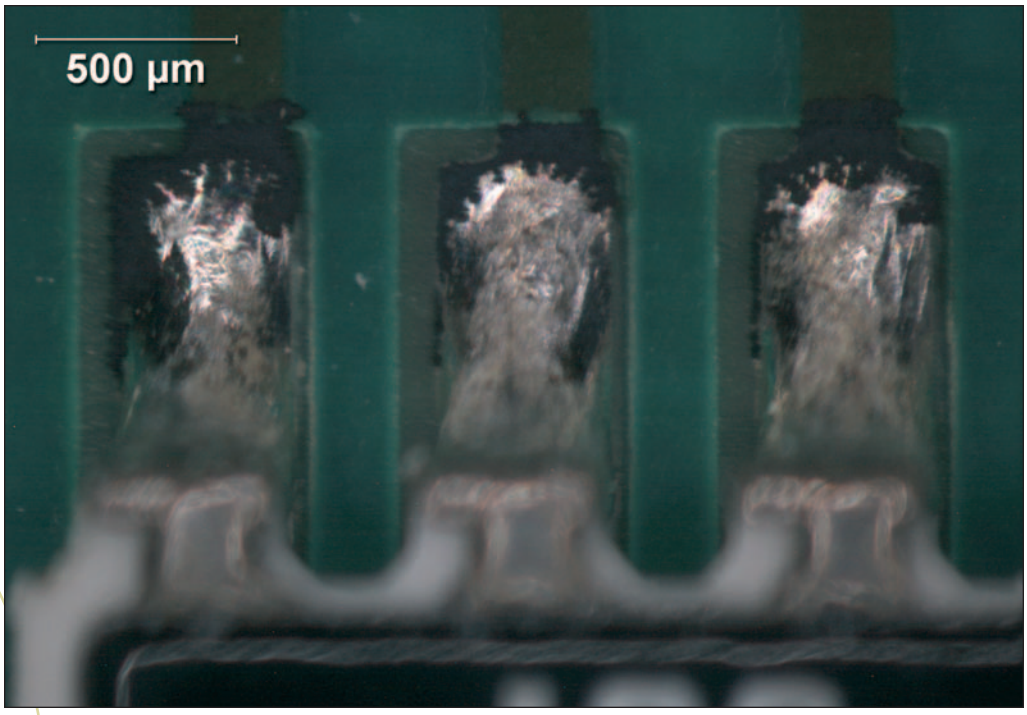


Figure 3-19: Image of black residue on multiple solder joints.

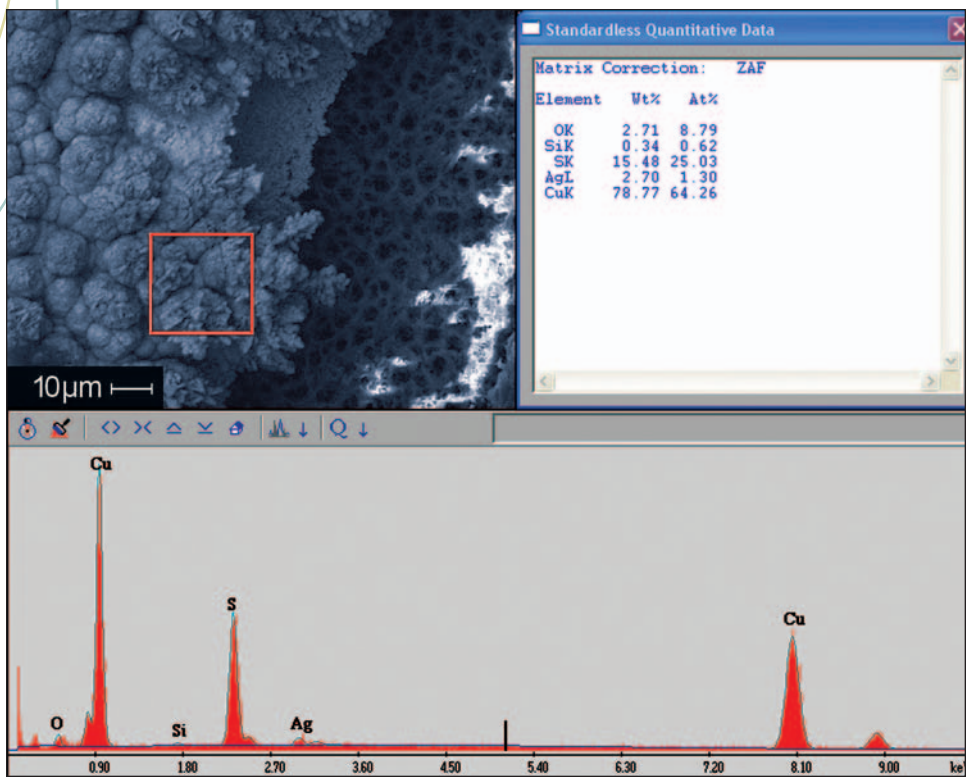


Figure 3-20: SEM-EDS data for the black residue showing sulfur corrosion.

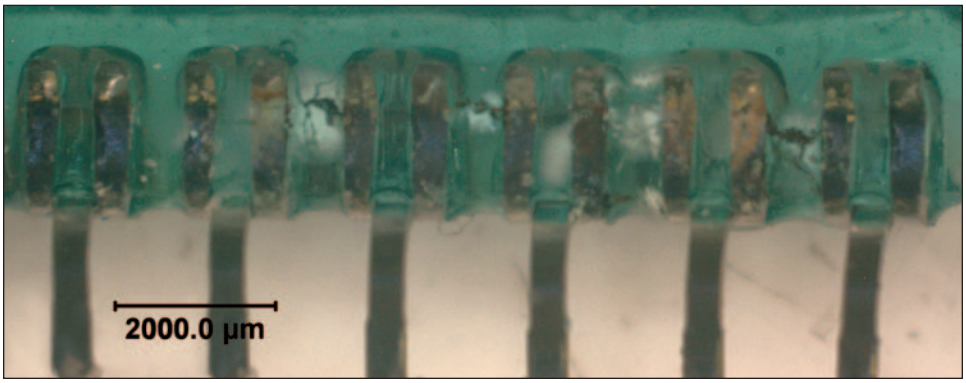


Figure 3-21: Uniform corrosion observed over all of the metallic surfaces.

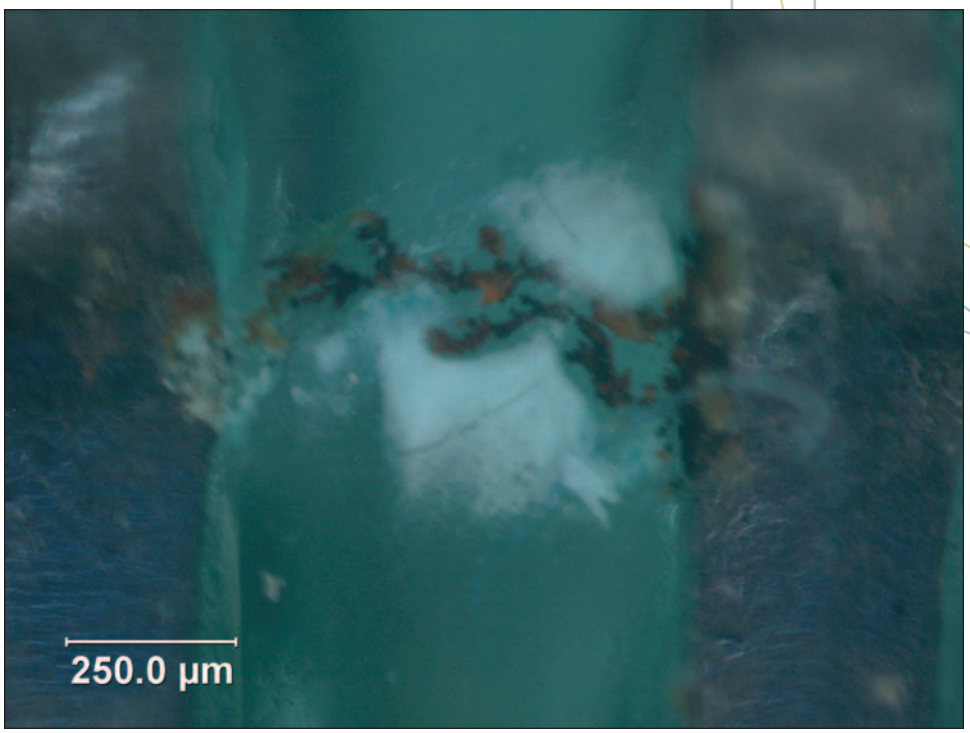
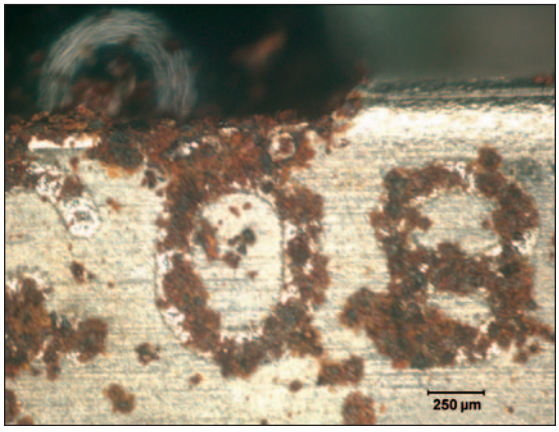


Figure 3-22: Image of a dendrite growing between two pins causing a short.



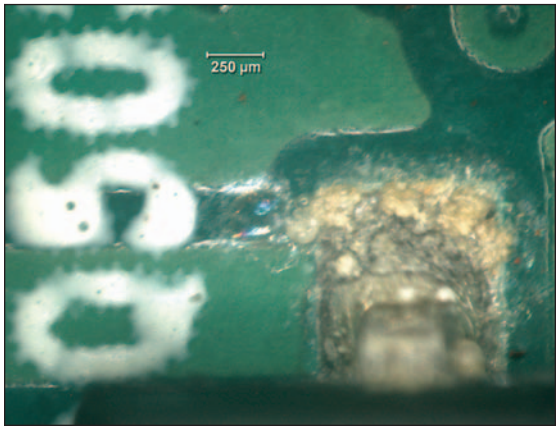


Figure 3-23: Images of the corrosion products on and around a component on an assembly with high activity residual flux.

4. Imaging

Microscopy and digital photography provide a permanent visual record of the sample, from the point of arrival to the laboratory through each step along the way in the determination of the root cause of the failure.

4.1. Automated Optical Inspection

Automated optical inspection (AOI) is used as a process tool for inspection of bare boards, solder paste deposition, component placement prior to reflow, post-reflow component conditions, solder joints, and surface anomalies on assemblies. By programming the features of a good board assembly, comparisons with subsequent assemblies can determine if they pass or fail.

4.2. Endoscopic Optical Inspection

An optical inspection system uses a lens placed very close to the board, nearly touching it, and a mirror directs the light path 90 degrees so that features to the right (or left) of the lens can be viewed. Fine features underneath components can be observed, especially the first two to five rows of a ball grid array (BGA) component. The row depth is dependent on the lighting and space beneath the component. The goal is to see if the solder balls have collapsed properly after undergoing the reflow process and if any abnormalities exist, such as contamination or materials bridging leads.

Figures 4-1 and 4-2 show solder ball shape variations, which are Process Indicator for Class 2 and 3: BGA solder ball terminations are not uniform in size, shape, coloration, and color contrast, per *IPC-A-610E, Section 8.3.12.3 - Surface Mount Area Array - Solder Connections*. Figures 4-1 illustrates that either the manual placement or the pick-and-place system was slightly off. Figure 4-2 shows solder ball size variation.

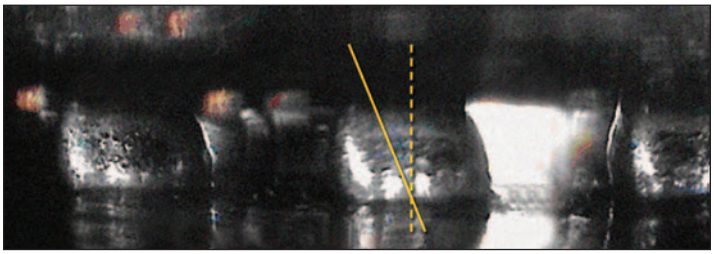


Figure 4-1: Image of a slight misalignment of a row of solder balls.

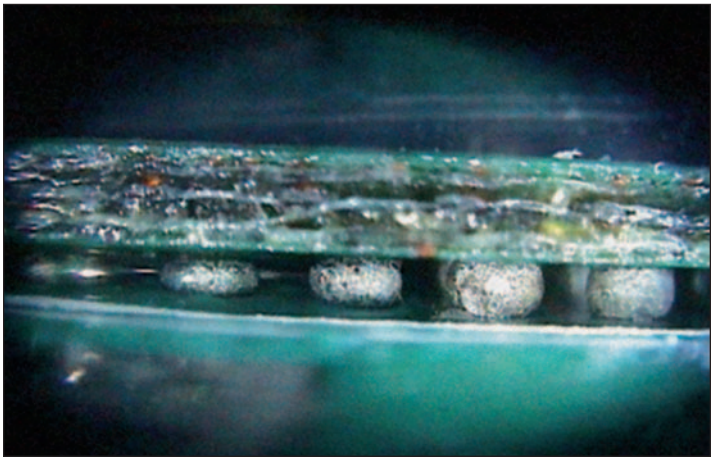


Figure 4-2: Image of the size variation of solder balls.

4.3. Optical Microscopy with Digital Imaging

A stereomicroscope is used in optical microscopy to give good depth of field when the sample is placed directly underneath the main lens. When used with calibration grids and the appropriate software, images can be captured with scale bars and measurements of features, at magnifications ranging from 7x to 90x. Figure 4-3 shows a partial fingerprint on an assembly that contributed to poor adhesion of a conformal coating.

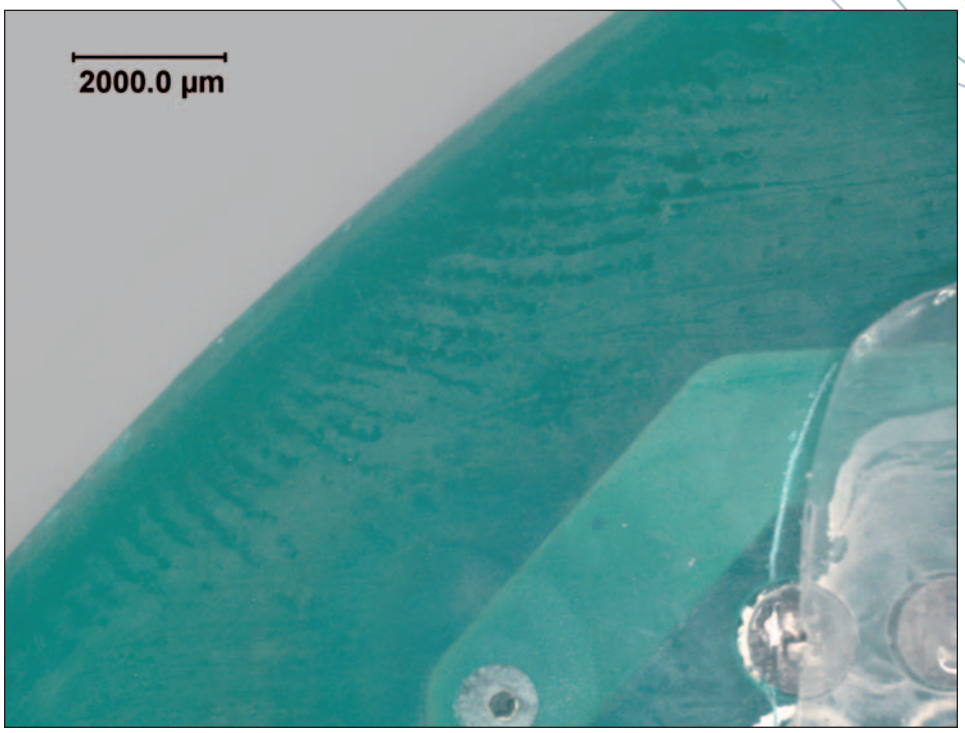


Figure 4-3: The oils from this fingerprint contributed to poor adhesion of the conformal coating and led to corrosion of unprotected metal surfaces.

4.4. Metallography with Digital Imaging

A stereomicroscope with an inverted stage is used to examine the structure and components of metals in microsectioned samples. When used with calibration grids and the appropriate software, images can be captured with scale bars and measurements of features, at magnifications ranging from 50x to 1000x. Figures 4-4 shows microsectioned solder joints as viewed on a metallographic microscope.

Figure 4-4: Metallographic images of solder joints.

4.5. Scanning Electron Microscopy with Energy Dispersive X-Ray Spectroscopy (SEM-EDS)

A scanning electron microscope (SEM) is a powerful imaging tool used for materials analysis and can be combined with energy dispersive X-ray spectroscopy (EDS), elemental characterization. The technique is typically destructive, since the sample chambers are smaller than most assemblies, but valuable information can be obtained about fracture surfaces, internal defects, diffusion, dimensional analysis, observing very fine features, and much more. When used with calibration grids and the appropriate software, images can be captured with scale bars and measurements of features, at magnifications ranging from 15x to greater than 70,000x.

Figure 4-5 shows SEM images of a decapsulated die which was found to have EOS damage.

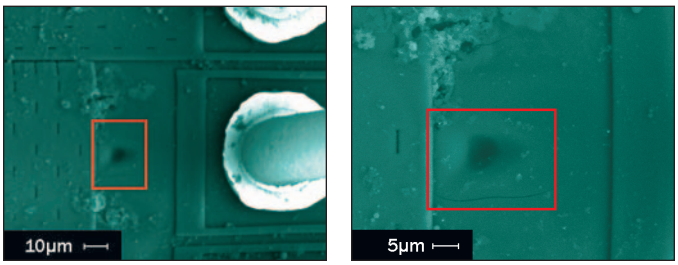


Figure 4-5: SEM images for EOS damage on a decapsulated die.

4.6. Transmission X-Ray Imaging and Inspection

X-ray inspection is used to visualize assemblies by observing differences in density and composition. The denser an item, the darker it appears in the image. Some of the features that can be observed are: cracks, solder joints, traces, vias, voiding within solder joints, and wire bonds.

This provides real time images and photographic evidence of good ball bonds. X-ray can be used to confirm the correct temperature profile for lead-free or lead SMT reflow processes by detecting the presence of voids in the solder balls.

Figure 4-6 shows an X-ray of a BGA component with bridging solder balls that were a result of improper solder paste printing. Figure 4-7 shows an X-ray of a damaged wire bond inside a component that was likely due to contamination from a corrosive residue.

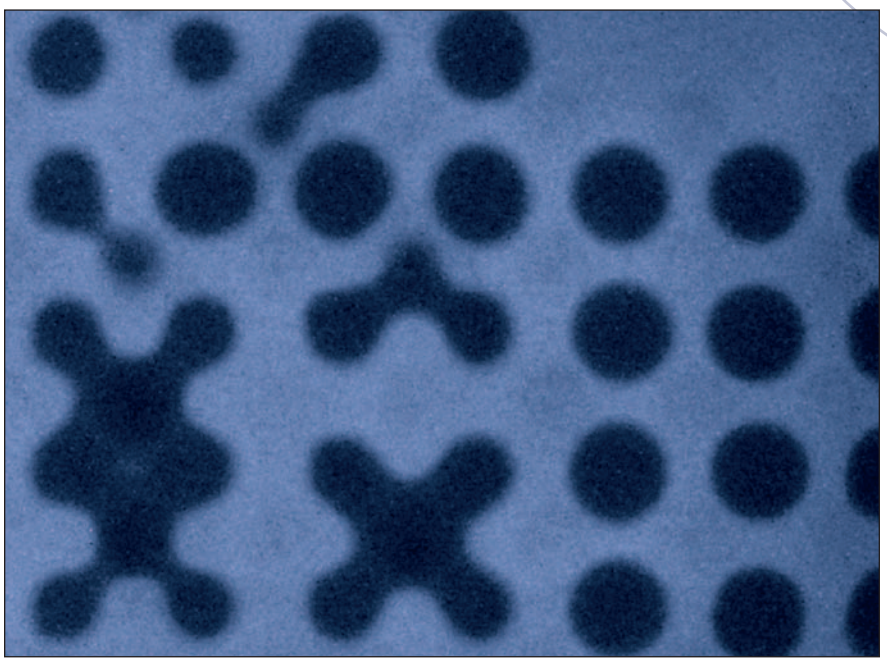


Figure 4-6: X-ray image of a BGA component with bridging solder balls.

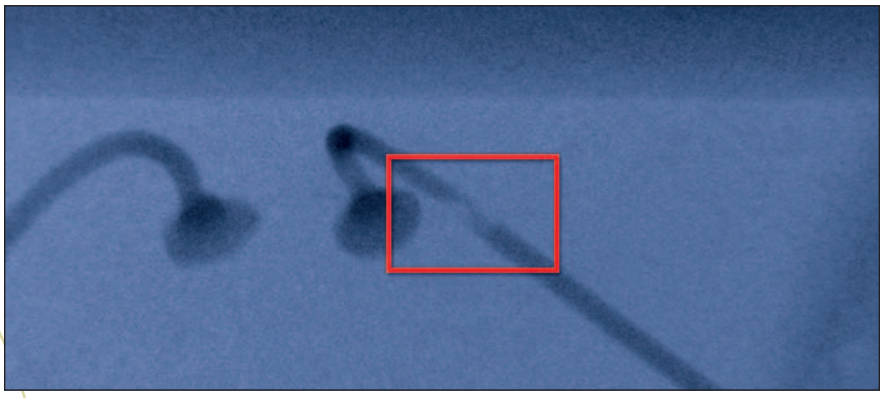


Figure 4-7: X-ray image of anomalous wire bond damage.

5. Cleanliness Testing

Ionic residues can lead to degradation of the electrical conductors via corrosion and/or dendrite formation, which can cause reliability issues. To determine if there are ionic contaminants present on a board, there are two methods that give different levels of information: Bulk Ionics Testing and Ion Chromatography. Organic contaminants can be identified using FTIR Spectroscopy, although complex mixtures may be difficult to resolve.

5.1. Bulk Ionics/Ionograph Testing

Bulk Ionics Testing, also known as Resistivity of Solvent Extract (ROSE), is performed with an Ionograph with the method in *IPC-TM-650 2.3.25C - Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract (ROSE)*, in which a sample is immersed in an isothermal bath (at 35ºC) containing a three to one solution of isopropyl alcohol to deionized water. Ionic contaminants extracted from the sample pass through a conductivity cell which continuously measures the conductivity of the solution. The conductivity values are integrated over the time of the extraction. The ionic material then passes through a deionization column before being recirculated back into the test chamber. As the ionic materials are extracted from the assemblies, the conductivity (and hence resistivity) of the solution will change dynamically until nearly all of the extractable ionic material has been removed.

Results from dynamic extraction by Ionograph are reported in micrograms of NaCl equivalent per square inch. For assemblies soldered using rosin based fluxes, the ionic cleanliness requirement per J-STD-001E is a maximum of 10.06 micrograms of NaCl equivalent per square inch (1.56 micrograms NaCl equivalent per square centimeter).

There is no industry standard for acceptable bulk ionic levels, but it is better to have as low a value as possible. ACI recommends Ionograph results to not exceed a level of two to three micrograms of NaCl equivalent per square inch.

5.2. Ion Chromatography

Ion Chromatography is a more specific method of ionic contaminant analysis as outlined in *IPC-TM-650 2.3.28A - Ionic Analysis of Circuit Boards, Ion Chromatography Method*, in which the samples are sealed in a KAPAK bag with a three to one solution of isopropyl alcohol to water and heated in an 80ºC water bath for one hour to extract any ionic residues. The extract solution is analyzed against known standards to confirm the presence of and quantify each of the following anions: fluoride, chloride, bromide, nitrate, phosphate, and sulfate in units of µg/mL. The surface area is calculated from the board dimensions and the final results are reported in µg/in^2.

ACI's maximum recommended amounts of fluoride, chloride, bromide, nitrate, and sulfate for bare boards are 2, 4, 5, 1, and 3 µg/in^2, respectively. The recommended levels of ionic contamination for populated assemblies will depend upon the application. However, for typical component packages on FR-4 or a like substrate, the maximum recommended amounts of fluoride, chloride, bromide, nitrate, and sulfate are 2, 9, 15, 1 and 10 µg/in^2, respectively. Both sets of acceptance criteria were developed from experience and in conjunction with industry leaders.

Figure 5-1 shows an ion chromatograph for an anion standard solution containing fluoride, chloride, bromide, nitrate, phosphate, and sulfate anions.

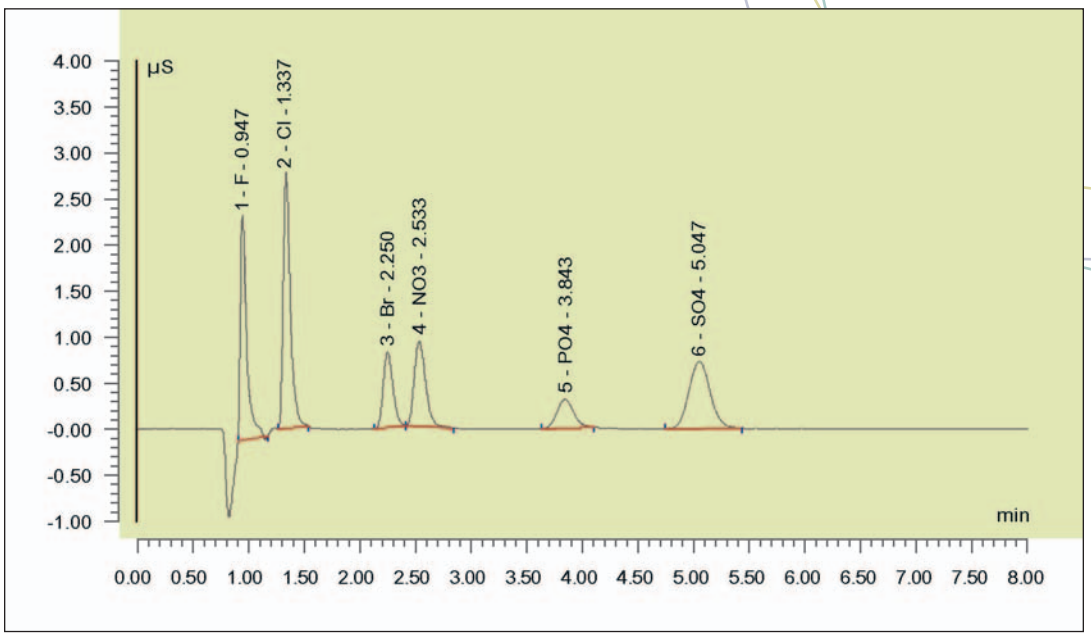


Figure 5-1: Example of an ion chromatograph, featuring a standard solution containing fluoride, chloride, bromide, nitrate, phosphate, and sulfate anions.

5.3. Residual Rosin Testing

Ultraviolet/Visible (UV/Vis) spectroscopy is used to quantify the residual rosin left from solder paste and/or wave soldering flux after the reflow and cleaning process per the method in *IPC-TM-650 2.2.27 - Cleanliness Test - Residual Rosin*.

5.4. Surface Organic Contamination Detection Testing

In accordance with *IPC-TM-650 2.3.38C - Surface Organic Contaminant Detection Test*, PCB samples are rinsed in a drop-wise fashion with 0.5 mL of acetonitrile onto pre-cleaned aluminum coated glass slides. Using aluminum coated glass sample slides instead of glass-only slides reduces the background infrared absorption from the glass itself, increasing the signal to noise in the subsequent analysis. After the solvent has evaporated, more acetonitrile is rinsed over the PCBs and evaporated. This process is repeated until a total of 3.0 mL of acetonitrile has been deposited and evaporated from the slides. A control slide is used to verify that no residue was left by acetonitrile alone.

The slides are examined for visible signs of residue. When residue is observed, images of the slides are captured using a microscope, as shown in Figure 5-2, and analyzed with the subsequent FTIR testing procedures.

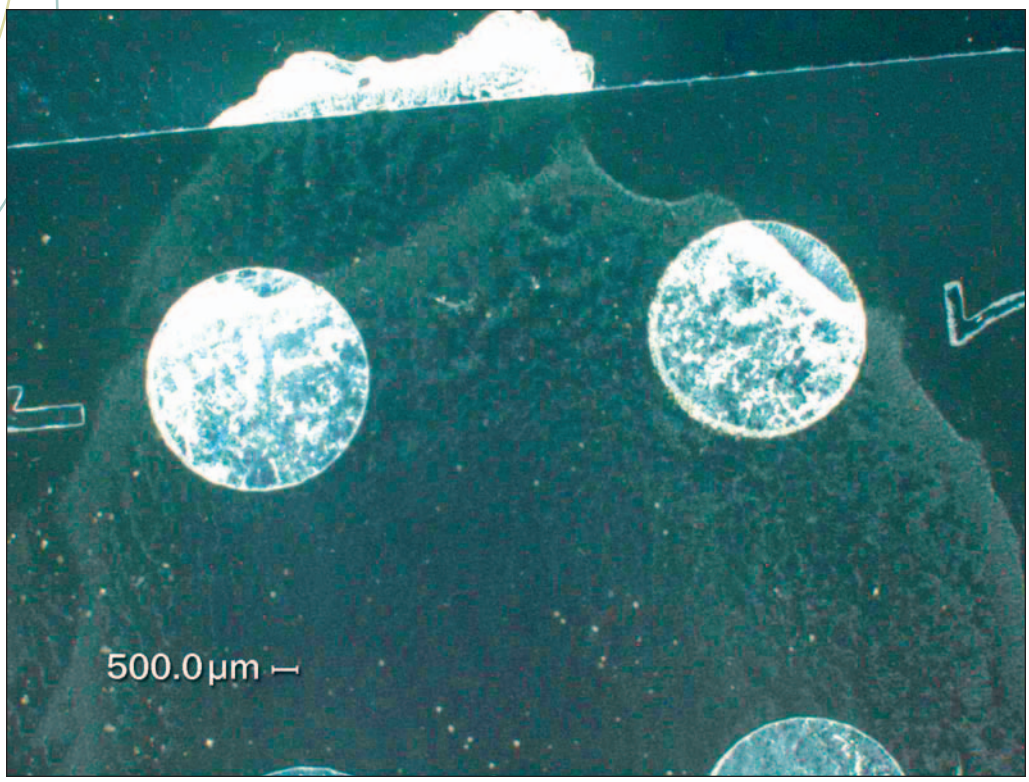


Figure 5-2: Image of residue obtained from rinsing a bare PCB.

5.5. Surface Organic Contamination Identification Testing

When residue is observed, the identity of the organic contaminant via Fourier Transform Infrared (FTIR) spectroscopy, is performed via the method outlined in *IPC-TM-650 2.3.39C - Surface Organic Contaminant Identification Test (Infrared Analytical Method)*.

The slides with residues are examined with an ATR-FTIR microscope to attempt to identify the composition of the residues. A background spectrum is run prior to capturing the spectra of all samples.

Figure 5-3 shows the FTIR spectrum of the residue rinsed from a board, as observed in Figure 5-2. Figure 5-4 shows the FTIR spectral comparison of the residue with that of a known adhesive.

5.6. Surface Insulation Resistance (SIR) Testing

The goal of surface insulation resistance (SIR) testing is to catch dangerous propensities for electrochemical failure mechanisms, such as unacceptable electrical leakage under humid conditions, corrosion or metal migration, before they can occur on produced assemblies.[7] SIR testing is one of the requirements in the *IPC-CC-830B - Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies* and is used as a replacement for the deactivated *MIL-I-46058 - Insulating Compound, Electrical (For Coating Printed Circuit Assemblies). MIL-STD-2000A - Standard Requirements for Soldered Electrical and Electronic Assemblies* requires SIR testing on conformally coated samples.

[7] Douglas O. Pauls, IPC Technical Activities Executive, Chairman of IPC Cleaning & Coating Committee & Senior Process Engineer, Rockwell Collins.

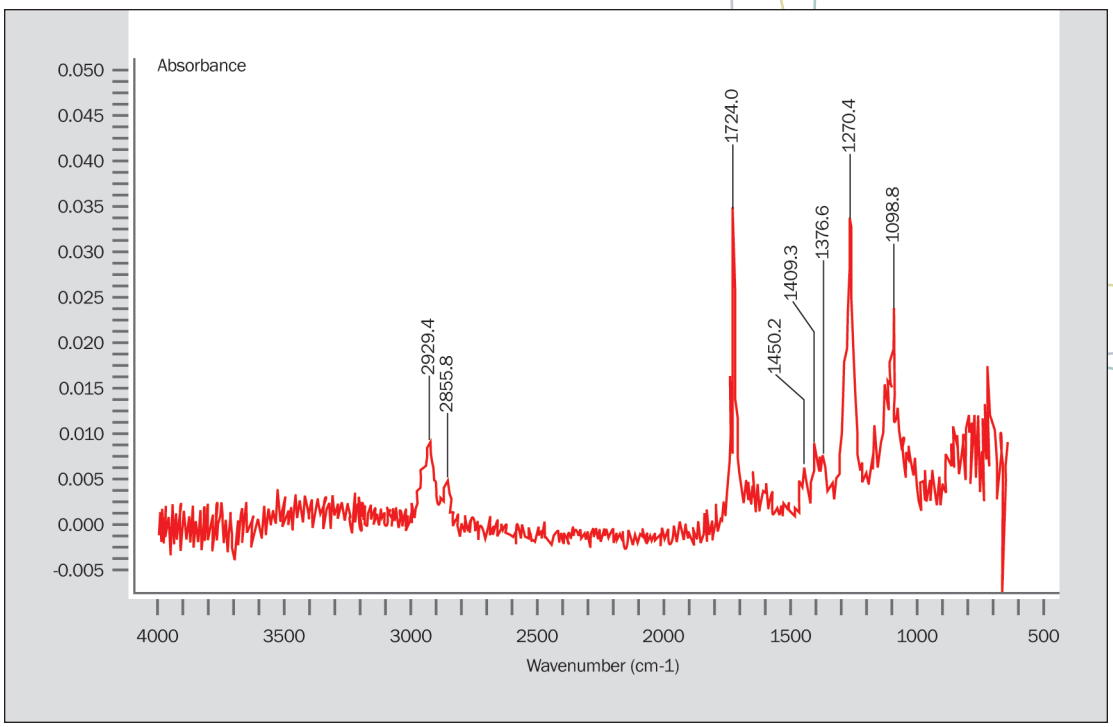


Figure 5-3: FTIR spectrum of residue rinsed from a PCB.

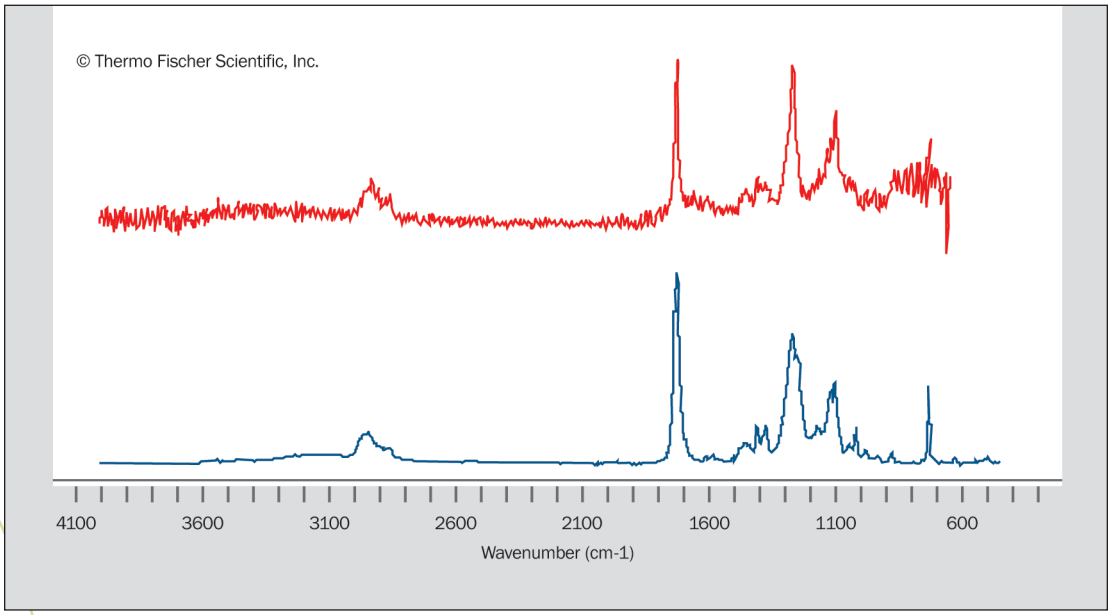


Figure 5-4: FTIR spectra compared for the residue from the PCB (top, red) with a known adhesive compound (bottom, blue).

6. Solderability Testing

Solderability is fundamental to electronics manufacturing, since it is required for metals to form structurally sound and reliable connections.

6.1. Accelerated Steam Aging

Accelerated steam aging is used to reduce the amount of time required to grow the oxides on surface finishes, which may inhibit solderability and require the use of stronger fluxes.

6.2. Dip and Look

Component samples are dipped in flux and solder is applied by a wetting balance. Any residue flux is removed with isopropyl alcohol before final inspection with an optical microscope at a minimum of 10x unless otherwise stated. *J-STD-002C - Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires* requires that parts exhibit a continuous solder coating free from defects for a minimum of 95% of the critical area of any individual lead. Anomalies other than de-wetting, non-wetting, and pin holes are not cause for rejection.

6.3. Solder Float Test

Printed circuit board (PCB) samples are tested to *J-STD-003B - Solderability Tests for Printed Boards, 4.2.3 Test C - "Solder Float Test"*. This test involves sectioning areas from a PCB to provide board sections no larger than 1.97 x 1.97 inches. The layout of the board and number of boards provide precluded the ability to test the *J-STD-003B* minimum number of locations of 30.

Flux is applied to the board section and allowed to drain. The section is slid on to the molten solder surface (pot temperature 235ºC). The section is allowed to float on the surface for a maximum of five seconds. The sections are removed, cooled and examined. The surface features and plated through holes (PTHs) contained by fixtures and those near the trailing edge (3 mm from the edge) are not included in the examination.

The pass/fail criterion is that a minimum of 95% of the surfaces features tested shall exhibit good wetting. Solder shall fully wet the wall area of the PTHs and plug holes less than 1.5 mm in diameter to meet Class 1 and 2 reliability levels. Class 3 defines successful wetting if solder has risen in all PTHs wetting the hole-walls with no base metal exposed or the presence of non-wetting. In addition for PTHs, the solder must wet over the knee of the hole and out to the land around the top of the hole for PCBs with thickness less than 3.0 mm.

Figure 6-1 shows sectioned PCB samples with solderability that was poor for samples A, B, and C and acceptable for D.

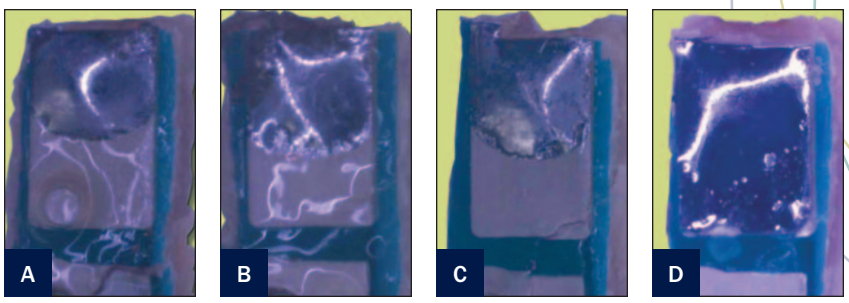


Figure 6-1: Images of solder wetting on sectioned board samples.

6.4. Wetting Balance

Wetting balance analysis involves dipping the pad areas into flux prior to applying solder using a wetting balance. Flux residue is removed post testing with isopropyl alcohol before final inspection at a magnification of 10x.

Acceptable solderability can be established through evaluation of wetting balance curve properties: wetting time, wetting force and general shape of the curve. *J-STD-003B* provides suggested evaluation criteria based upon these properties.

Figure 6-2 shows a typical and acceptable wetting balance curve with wetting just under one second at the crossover time and illustrating the buoyancy effect on the part, and the maximum wetting force.

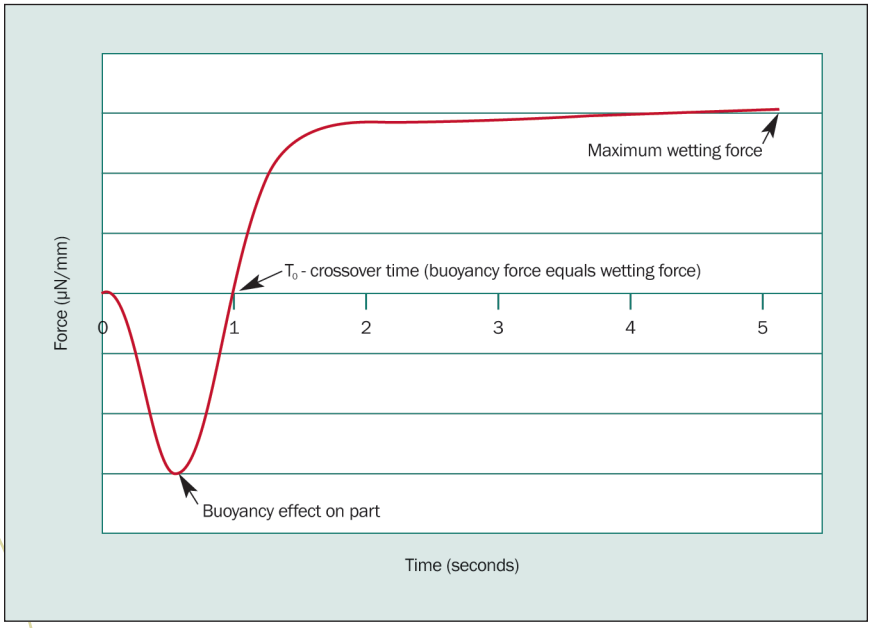


Figure 6-2: Wetting balance curve.

6.5. Sequential Electrochemical Reduction Analysis (SERA)

SERA can be employed only if the pads/holes are large enough (≥ 0.005 cm^2) and/or electrically connected to a second known accessible pad or trace.

In SERA analysis, a borate buffer solution is allowed to contact the pad/through-hole and a constant current is applied to the solution, converting any reducible species (i.e., metal oxides, metal sulfides, etc.). The measured voltage determines the nature of the oxide and the charge density (or time for reduction to occur) determines the thickness of the oxide layer.

Figure 6-3 shows a SERA graph for a copper foil sample that had cuprous oxide, cupric oxide, and cuprous sulfide layers on the copper substrate.

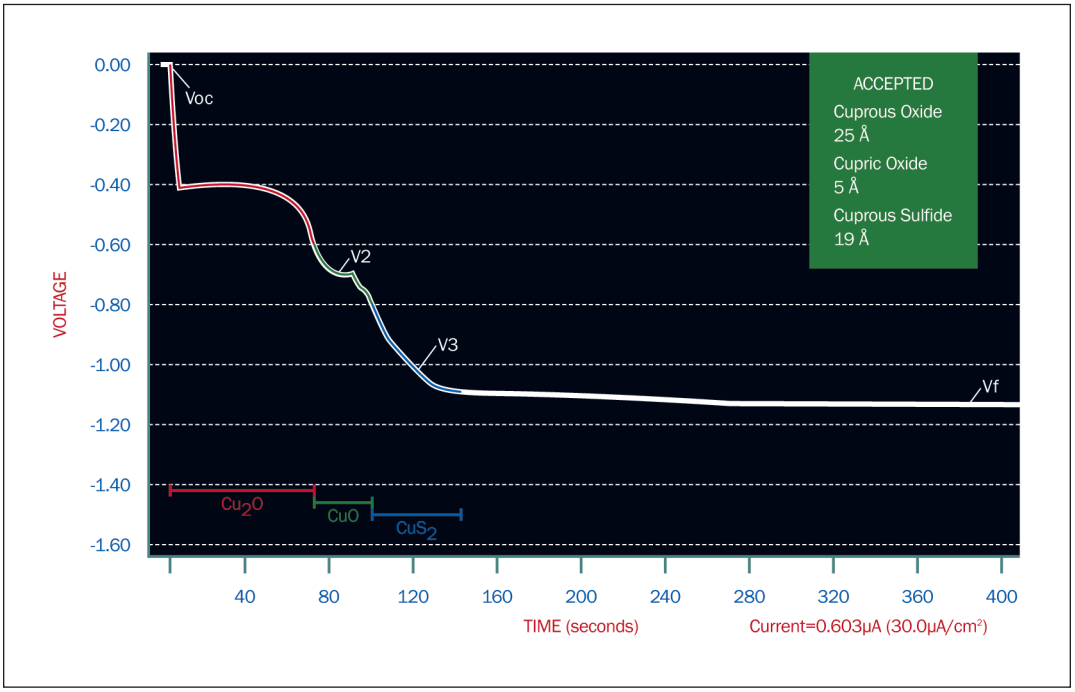


Figure 6-3: SERA data for a copper foil sample.

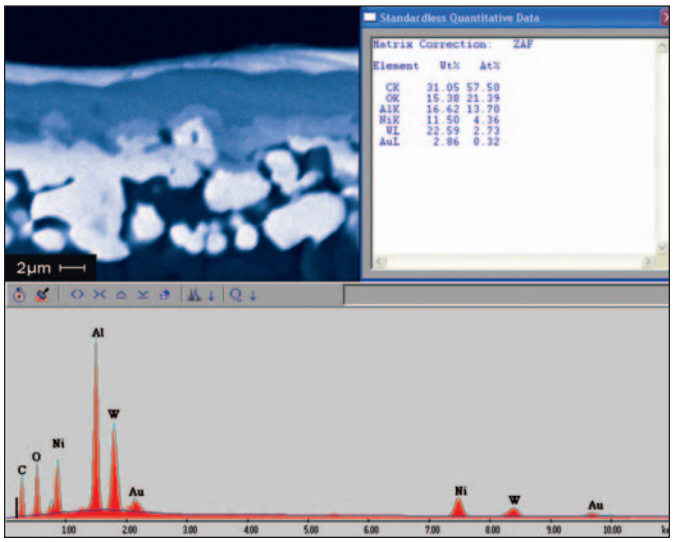
7. Spectroscopic Analysis

Spectroscopy involves the measurements of quantities as a function of frequencies or wavelengths, including how energy interacts with matter. These interactions provide information as to the identity and quantity of the composition of the matter.

7.1. Energy Dispersive X-Ray Spectroscopy (EDS)

EDS is used to evaluate the elemental composition of materials within a scanning electron microscope (SEM), exciting the sample with X-rays, and then measuring the energy levels of X-rays emitted, which are specific to each element. EDS provides the identity of the elements present in a sample, along with their amounts in weight percentage and atomic percentage concentrations.

Figure 7-1 shows the SEM-EDS data for the metallization on a ceramic component that has carbon (C), oxygen (O), aluminum (Al), nickel (Ni), tungsten (W), and gold (Au). Figure 7-2 shows SEM-EDS elemental mapping data for the same area, illustrating the fact there is a gold layer on top of a nickel plating layer which is on tungsten metallization.



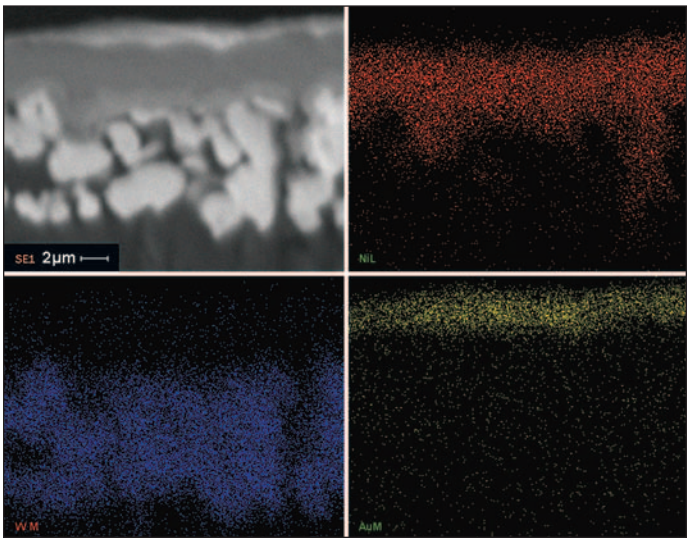


Figure 7-1 (left): SEM-EDS data for a ceramic component metallization of a QFN.

Figure 7-2 (right): SEM-EDS elemental map of a ceramic component metallization of a QFN. Top left - image, top right - nickel (red), bottom left - tungsten (blue), bottom right - gold (yellow).

7.2. Fourier Transform Infrared (FTIR) Spectroscopy

FTIR spectroscopy is a technique in which infrared energy is used to excite fundamental vibrational and associated rotational-vibrational modes of molecules in the mid-infrared, approximately 4000 to 400 cm^{-1}. These vibrational modes correspond to molecular structures. Attenuated Total Reflectance (ATR) is a technique used with FTIR, which allows liquid and solid samples to be studied directly without further preparation. In ATR-FTIR, an infrared beam is directed through an optically dense crystal at a certain angle and internally reflects through the crystal, producing evanescent waves. When the crystal is pressed against an infrared active material, the infrared radiation from the evanescent waves penetrates typically one to four micrometers into the sample. Figure 7-3 shows an FTIR spectral comparison of a potting material with poly(dimethylsiloxane).

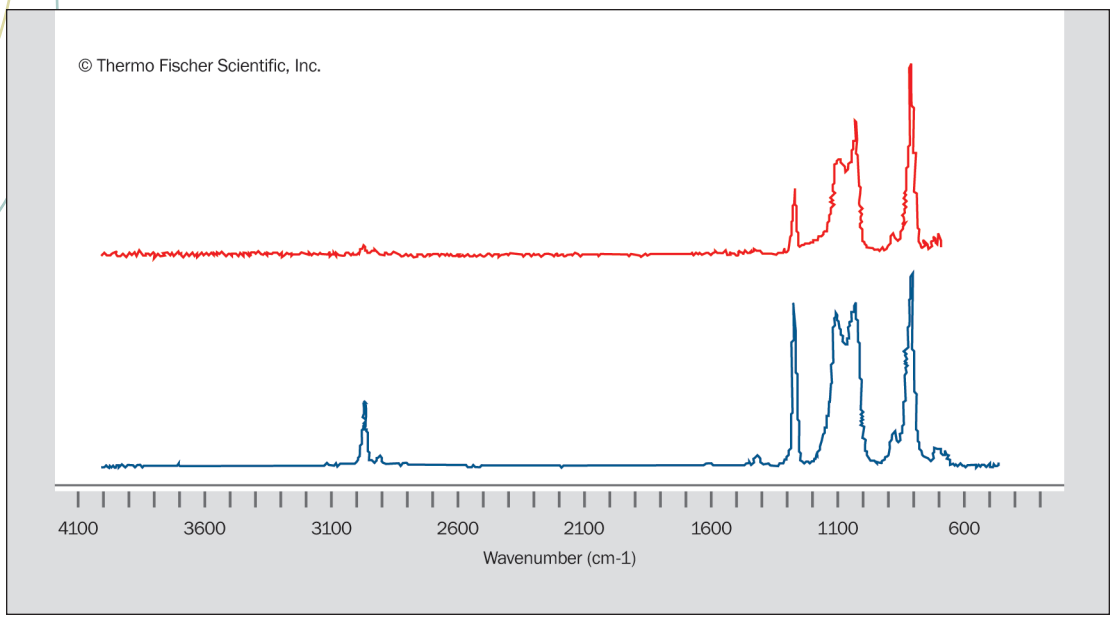


Figure 7-3: FTIR spectral comparison of potting material compared to poly(dimethylsiloxane).

7.3. Ultraviolet/Visible (UV/Vis) Spectroscopy

UV/Vis is used to measure electronic transitions of molecules in the ultraviolet to visible spectrum, approximately 180 to 800 nm. These transitions correspond to chemical structures which determine to amount of light energy absorbed, transmitted, and reflected, and can be used to characterize certain compounds and optical properties of materials. Figure 7-4 shows the UV/Vis transmission spectra of two types of coated glass samples.

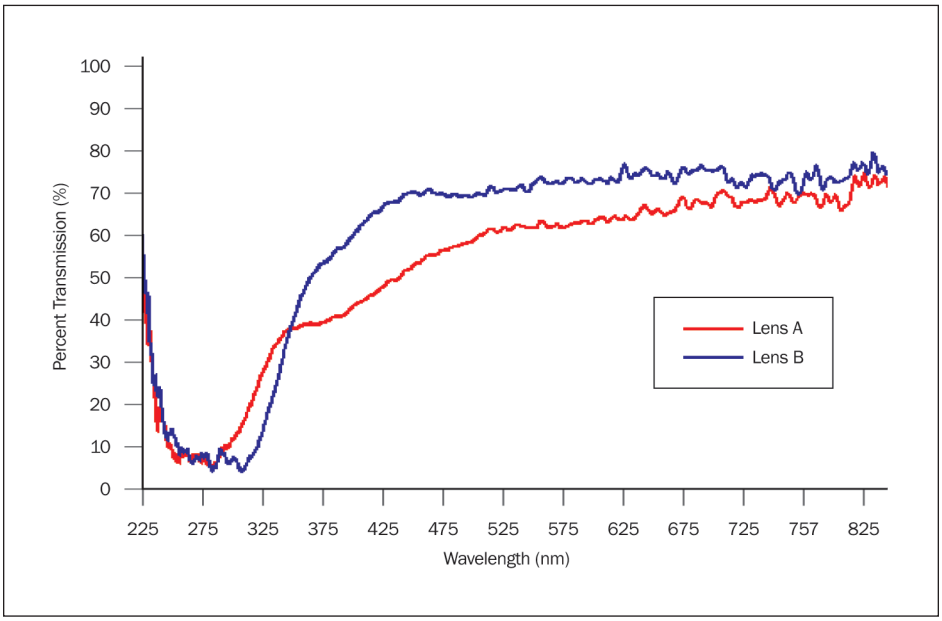


Figure 7-4: UV/Vis data for transmission properties of two types of coated glass.

7.4. X-Ray Fluorescence (XRF) Spectroscopy

X-Ray Fluorescence (XRF) is used to identify composition and plating thickness for elements ranging from titanium (Ti, element 22) to uranium (U, element 92). By bombarding a sample with high energy X-rays, "secondary" (or fluorescent) X-rays can be emitted which are characteristic of the atoms present in the sample. Figures 7-5 and 7-6 show XRF spectrum of ENIG surface finish and a tin-lead solder joint, respectively.

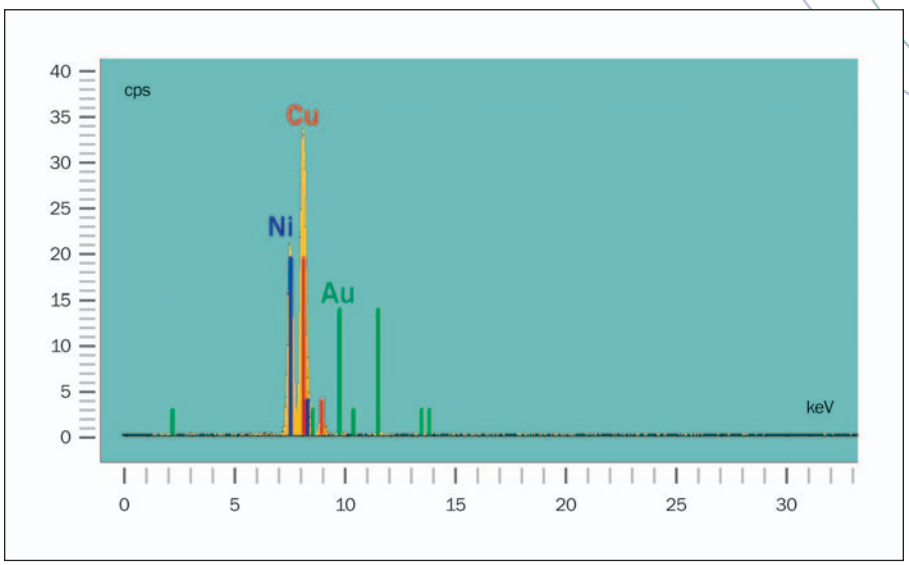


Figure 7-5: XRF spectrum of an electroless nickel immersion gold (ENIG) surface finish over copper, where copper (Cu), gold (Au), and nickel (Ni) were observed.

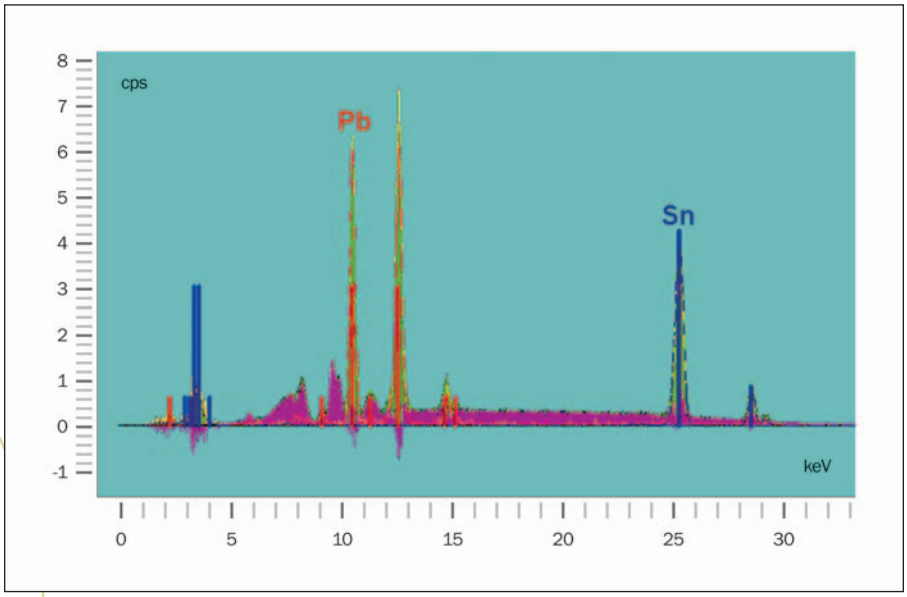


Figure 7-6: XRF spectrum of a tin-lead solder joint, where lead (Pb) and tin (Sn) were observed.

8. Thermal Analysis

Thermal analysis involves measurements of heat or thermal energy and its interaction with matter. The amount of energy transferred into or out of the sample gives fundamental information about the properties of that material.

8.1. Differential Scanning Calorimetry (DSC)

DSC is used to measure the difference in the amount of heat required to increase the temperature of a sample and reference as a function of temperature. DSC is used in studying phase transitions of materials, such as melting, glass transitions, and exothermic decompositions. These transitions involve energy changes or heat capacity changes that can be detected with great sensitivity by DSC.

Figure 8-1 shows an example of a DSC curve of the melting endotherm of a pure sample of phenacetin (p-acetophenetidide).

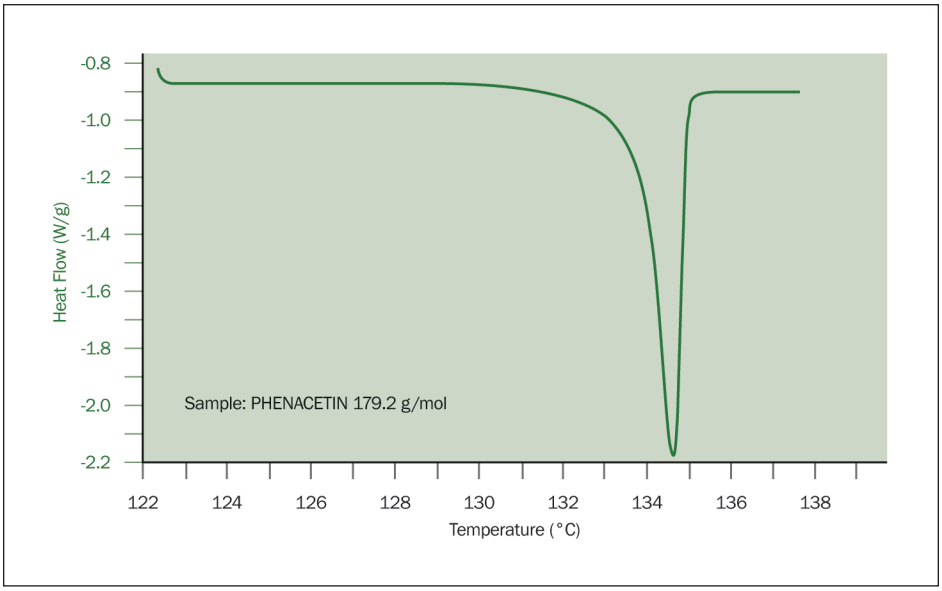


Figure 8-1: DSC melting curve of a pure sample of phenacetin.

8.2. Thermal Gravimetric Analysis (TGA)

TGA is used to measure changes in weight of a sample in relation to changes in temperature. TGA is used in research and testing to determine characteristics of materials such as polymers, to determine degradation temperatures, absorbed moisture content of materials, the level of inorganic and organic components in materials, and solvent residues.

Figure 8-2 shows a TGA curve of the decomposition of calcium oxalate monohydrate ($CaC_2O_4 \cdot H_2O$) that exhibits three weight losses with temperature in an inert atmosphere. The three levels appear to represent the loss of water, carbon monoxide and carbon dioxide via the process shown in Figure 8-3.

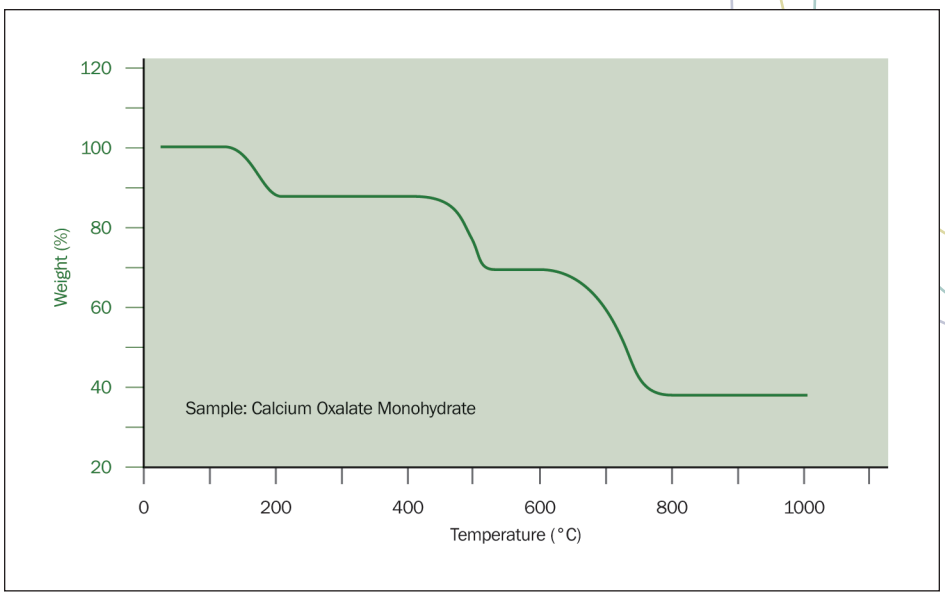


Figure 8-2: TGA curve of the thermal decomposition of calcium oxalate monohydrate.

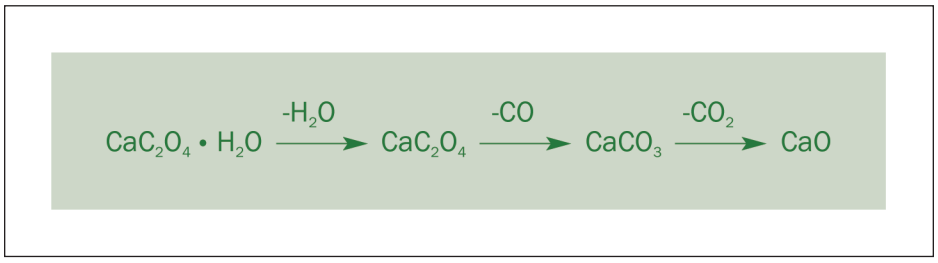


Figure 8-3: Chemical decomposition of calcium oxalate monohydrate to calcium oxide.

9. Wire Bond Mechanical Testing

Wire bond mechanical testing is necessary for determining the quality of the wire bond connections within a microelectronics device.

9.1. Ball Wire Bond Shear Testing

A ball wire bond shear is a destructive test which determines the strength of a ball wire bond. A constant horizontal force is applied to the side of the ball wire bond until the wire bond weld fails. The breaking force of the ball bond is recorded. The breaking force of the bond must be correlated with its ball diameter for proper assessment of its ball shear strength. The shear breaking force is generally expressed in grams-force per area. ACI has ball wire bond shear testing capabilities up to 5000 grams-force.

9.2. Wire Bond Pull Testing

A wire bond pull test is a destructive test which determines the strength and quality of the wire bonds. A constant upward force is applied to the wire via a hook placed under the wire and the force at which the wire bond fails is recorded. The breaking forces are generally expressed in grams-force. Along with the breaking force, the mode of failure is also recorded. Method 2011.7 of *MIL-STD-883* provides specifications for acceptable minimum wire pull strengths. ACI has double bond wire pull capabilities up to 1000 grams-force.

9.3. Non-Destructive Wire Bond Pull Testing

Method 2023.5 of *MIL-STD-883*[8] provides for a Non-Destructive Bond Pull, where an applied stress (measured in grams-force (gf) pull) is used to reveal non-acceptable wire bonds while avoiding damage to acceptable wire bonds in a package. This test is intended for "Class S" parts or parts intended for use in the high reliability space flight community.[9] Any bond failures are unacceptable, but based on the program requirements, rework and retest may be acceptable. Specifications are provided prior to testing, such as the allowable stress, which sets the maximum amount of grams force to be applied. The wire bond passes if it survives up to that limit.

9.4. Die Shear Testing

Die shear testing is a destructive test which determines the adhesive strength of attached die. A constant horizontal force is applied to a side of a die until the die adhesion fails. The breaking force required for adhesion failure is recorded. The breaking force should be correlated to the area of the die for proper assessment of the adhesion strength. The die shear breaking force is generally expressed in grams-force per area. ACI has die shear testing capabilities up to 100,000 grams-force.

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[8] "Test Method Standards, Microcircuits." MIL-STD-883, <http://www.dscc.dla.mil/Programs/MilSpec/listdocs.asp?BasicDoc=MIL-STD-883>.

[9] "Assurance Issues Related to Electronic Wire Bonds." NASA Goddard Space Flight Center, <http://nepp.nasa.gov/wirebond/>.

10. Non-Destructive Testing

Failure analysis (FA), by its very nature, is needed only when things go awry. Before any testing is performed on the sample, a decision must be made as to whether or not the sample is allowed to be destroyed in the process of testing. Non-destructive testing can allow for re-use of the assembly since the functionality is not altered, but there still remains the possibility that inadvertent damage can occur through the course of the analysis. If non-destructive testing is preferred, then the following types of analysis can be performed. The testing can be divided into three categories: visual, X-ray (X-ray imaging and X-ray fluorescence), and mechanical (non-destructive wire bond pull).

The following types on non-destructive testing are available at ACI and have been described previously.

10.1. Cleanliness Examination

- Bulk Ionics/Ionograph Testing
- Ion Chromatography
- Surface Organic Contamination Detection Testing
- Surface Organic Contamination Identification Testing

10.2. Visual Examination

- Automated Optical Inspection
- Endoscopic Optical Inspection System
- Optical Microscopy with Digital Imaging

10.3. X-Ray Examination

- Transmission X-Ray Imaging
- X-Ray Fluorescence (XRF) Spectroscopy

10.4. Mechanical Examination

- Non-Destructive Wire Bond Pull Testing

11. Counterfeit Component Screening

ACI provides counterfeit component screening to assist customers in verifying that products are as they claim to be.

There exists a growing problem of counterfeit components entering the global supply chain. In recognition of the unique needs of the distribution and manufacturing community, ACI offers analysis of the parts inside two business days. This allows the customer the time to make any financial or production decisions. This service is ideal for independent distributors, franchised distributors, OEMs, CMs and anybody who needs verification that the product received is as it is represented to be. For best results, samples should be submitted with the data sheet and have the same date and lot codes with a maximum of five samples at a time.

Services offered:

- Inspection of suspected counterfeit components to the *IDEA-STD-1010-A Standard*.

Analysis includes:

- Visual and Mechanical Inspection
  - All microscopy services
  - Lead integrity analysis
  - Marking removal analysis (black topping, laser marking, chemical washing)
- Solvency Testing to Determine Marking Permanency
  - Date code changes/lot code changes
  - Marking verification (part numbers, logos, ink marks)
  - Detection of simulated laser markings
  - Lead-free remarking
- X-Ray Analysis
  - Internal component inspection
  - Lead-free analysis of Restriction of Hazardous Substances (RoHS) Directive compliant parts

12. Solder Analysis

ACI provides solder content analysis for solder pot samples for determining the level of contamination within the solder pot.

Samples of a customer's solder pot are analyzed spectrographically to determine concentrations for the following elements: arsenic, antimony, gold, iron, nickel, bismuth, aluminum, copper, silver, zinc, cadmium, indium, sulfur, and phosphorus, in addition to tin and lead. These measurements are compared against an industry standard, *IPC- J-STD-001E*.

This solder analysis service is used to assure that the solder pot has not become contaminated. Periodic testing will insure the correct balance of tin-lead (SnPb) for SnPb solders and the correct balance of metals in lead-free solders. Maintaining proper metal levels in the solder bath will reduce production rejects.

The solder pot can become contaminated from component finishes leaching into the solder pot, from improper maintenance of the solder pot, or from poor operator training. For example, an operator may mistakenly scrape SnPb solder splash and/or put a SnPb solder bar into a lead-free solder pot. Two SnPb solder bars are enough to raise the lead content of an 800 pound lead-free solder pot over the 0.1% RoHS directive limit.

Impurities can affect melting point, solder tension, and wetting of the solder. Typical production defects possibly resulting from contaminated solder pots are icicling, bridging, pin-holing, webbing, and poor joint connections. To gain control of contamination in wave soldering, ACI recommends performing solder alloy analysis on a weekly basis to determine the rate at which the solder pot becomes contaminated. After two to three months of gathering data, the solder pot analysis may be reduced to once a month, depending on usage and the rate at which the solder pot is contaminated.

Printed circuit board fabricators and assemblers are assured of high quality solder in the pot, constantly kept within specification ranges. Rates of rejection are reduced, thereby creating a more cost-effective and profitable manufacturing process. Many other solder manufacturers provide analytical services, but often charge the customer and take at least a week to provide analytical results. In the meantime, if the pot is contaminated, a week's worth of production using contaminated solder may result.

13. Environmental Stress Screening (ESS) Testing

Environmental testing is critical to ensuring the reliability of a product. Whether it's accelerated testing, component/PWB qualification, reliability tests or burn-in, ACI's environmental testing laboratory can assist with test planning, execution, and data analysis. In-situ data acquisition and custom fixturing is also available.

13.1. Highly Accelerated Stress Testing (HAST)

The 15" x 15" x 15" HAST chamber has a maximum temperature of 143ºC, a relative humidity level controlled between 75% and 98%, and a pressure in the range of 0.02 to 0.2 MPa (~2 atm maximum). Testing is performed to *JESD22-A110-B* and others.

13.2. Mechanical Drop Shock Testing

The drop shock test system is customized with a dual mass shock amplifier which can achieve impact forces up to 25,000 g for events as short as 0.25 milliseconds in duration. The equipment configuration can be adjusted to adjust the force waveform profile to meet testing needs with a piezoelectric accelerometer is employed to accurately measure acceleration forces for events. Custom fixturing can be designed to position test vehicles of a variety of sizes within a 9" x 9" footprint and along all three axes of orientation. In addition to performing a wide variety of programmable drop shock tests, the system can also perform materials impact evaluation (cushion testing) by dropping a load mass onto a fixed stationary object.

13.3. Salt Fog Chamber Testing

Salt fog chamber testing provides a controlled salt environment that measures 24" x 18" x 30". Testing is performed to the following standards: *ASTM B-117*, *MIL-STD 883E 1009.8*, *MIL-STD 810E*, *JESD22-A107-A*, and others.

13.4. Temperature/Humidity Cycling

Samples are exposed to environments of specified temperature and humidity, such as the commonly used 85ºC and 85% relative humidity condition. Testing is performed to *MIL-STD 810E*, Method 507.3 and others.

13.5. Thermal Cycling

Thermal cycling can be performed in multiple chambers from -65 to 155ºC with a maximum ramp rate of 10ºC per minute. Humidity control is also available. Testing is performed to *MIL-STD-883E 1010.7*, *JESD22-A-104-B* and others.

13.6. Thermal Shock

Thermal shock can be performed from -75 to 160ºC with a switching time of less than five seconds. The chamber sample holder is 3.5" x 9" x 11". Testing is performed to *MIL-STD 883E 1011.9*, *MIL-STD 810E 503.3*, *JESD22-A-106-A*, and others.

13.7. Vibration/Mechanical Testing

Vibration/mechanical testing can be performed with sine wave vibration, sine-sweep vibration, and random vibration tests. The frequency ranges are two to 6,500 Hz for sine wave and sine sweep vibration and two to 2,000 Hz for random vibration. The vibration can mechanically stress various sample configurations, up to 30 pounds horizontal load at 3.2 g peak or 10 pounds vertical load at 10 g peak.

14. Summary

ACI Technologies offers a full range of product support services tailored for the electronics manufacturing industry. ACI provides a competitive advantage with its wide range of technical expertise in chemical, electrical, materials, manufacturing, and mechanical engineering. ACI's talented technical staff is available on-demand to support your electronics manufacturing needs.

The analytical services laboratory aids in solving a variety of industry concerns including materials testing, cleanliness analysis, solderability testing, and failure analysis of printed wiring assemblies and electronic components. In addition to routine analysis, ACI also examines problems in-depth, utilizing a team of experienced scientists and engineers to perform detailed investigations, including on-site process audits. Once an analysis is completed, a preventative course of action is recommended, such as: incoming inspection, vendor qualification, process development, quality control improvement, and final assembly inspection.

ACI's core competencies in engineering, R&D, manufacturing, analytical services, and training courses in electronics manufacturing are readily available for immediate implementation to assist your organization in delivering a quality product.

Figure 14-1: ACI Technologies' manufacturing factory floor is equipped with the latest technology for building, repairing, reworking, testing and analyzing electronic circuit assemblies.

15. About the Author

Sean Owen Clancy, Ph.D. is a Research Associate/Chemist at ACI Technologies, Inc. He received his Ph.D. degree in Chemistry from the University of Southern California, Los Angeles, California.

He has more than fourteen years of experience in product development and materials analysis in academia, government, and commercial groups in advanced technology industries. He has more than six years of experience and a proven track record of project management, creating and leading technical teams, writing and editing technical publications and funding proposals for government agencies, providing instruction, and business development.

He brings to ACI over three years of experience in organic electronics in the areas of conjugated heterocyclic polymers for charge storage applications and aqueous analyte electrochemical sensors via functionalized carbon nanotube-based devices. In graduate school, his research focused on the synthesis and photophysics of visible and near-infrared light emitting polymer-lanthanide complexes. Prior to graduate school, he synthesized medicinal compounds for two years at Mayo Clinic Jacksonville. He has strong technical skills and hands-on experience in creating or modifying existing products and processes using analytical, synthetic organic, and polymer chemistry, as well as materials science.

Figure 15-1: Sean Clancy is among the highly qualified personnel at ACI available to perform the necessary analysis and testing to resolve electronics manufacturing issues.

16. Services and Training Overview

Meeting all of your electronics manufacturing needs and providing solutions through exceptional analytical laboratory, design, and manufacturing factory services. ACI Technologies also provides IPC and custom training with value added failure analysis and manufacturing discussions, as well as equipment demonstrations, ensuring students receive a training experience that exceeds their expectations.

Analytical Laboratory Services

- Cleanliness Testing and Contamination Analysis
- Component Qualification
- Counterfeit Components Screening
- Failure Analysis and Reliability Testing
- IPC Standardized Testing
- FTIR and UV-Vis Spectroscopy
- Materials Analysis
- Printed Wiring Board Qualification
- SEM-EDS Analysis
- Solderability Analysis
- X-Ray Fluorescence (XRF) Spectroscopy
- X-Ray Inspection

Design Services

- Analog and Digital Designs
  - Mechanical Design
  - Power Electronics System Design
- Component Engineering
- Design and Product Development
- Design for Manufacturability Analysis
- Engineering Design, Sustainment, Reverse
- Obsolescence Mitigation
- Systems Engineering
- Thermal Analysis of Electronics

Manufacturing Factory Services

- Chip Scale Manufacturing
- Design for Manufacturability and Testability (DFM, DFT)
- Flying Probe Testing
- Independent Vendor Survey and Qualifications
- Lead Free Manufacturing Process Development
- Manufacturing Engineering Services
- Manufacturing Process Development Support
- Rapid Prototyping and Pre-Production Builds
- Rework and Repair (BGA, CSP, PCB)

Training and Workforce Development

- Boot Camp: A hands-on, comprehensive course covering the complete electronics manufacturing process.
- Customized Curriculum Development
- Electronics Manufacturing Skills Based Courses
- IPC Certification Courses
- Lead Free Manufacturing
- Master Certified Instructors
- On-Location Options: Instructors come to you.
- Online Courses
- Secure Online Registration

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